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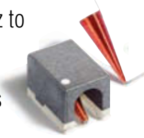

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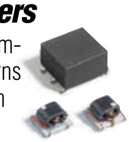

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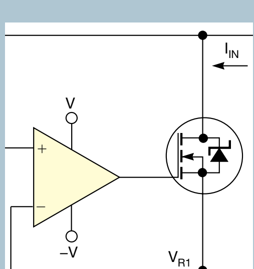

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DEPARTMENTS & COLUMNS

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Volume 56, Number 14 (Printed in USA).

BY PATRICK MANNION, DIRECTOR OF CONTENT

The shuttle program is over: What's next?

Recently, while reading *The New York Times*, I came across yet another mournful paean to the last space-shuttle flight. Despite my better judgment, I read it and gagged on my bottled water. Here's what made me gag: In the letter to the editor, the writer stated that "the mysteries we uncover in outer space will … give us a better sense of our purpose in this vast and largely empty universe." The letter writer then turned to the usual nice fallback of why we should stop making scopes for weapons and start making telescopes instead (**Reference 1**). Does anyone really believe our sense of purpose will come from out there? I don't. It lies right here.

Now, don't get me wrong. As a techie, I can think of few more inspiring achievements than the first moonwalk and am well-aware of the many advances that were by-products of that great adventure. I've got my autographed Buzz Aldrin books, and I've been to every space museum I can find. Just last week, on a clear night, my son and I lay back and just looked at the stars in sheer amazement and wonder.

However, I also recently read another article, from which I learned that President Obama is walking out of meetings just as the United States, with more than $14 trillion of debt, is about to default on its loans (**Reference 2**). Just before reading these articles, I had taken a cab to the San Francisco International Airport. During the ride, the driver talked about the fact that only 60% of students in Oakland, CA, graduate from high school and that most of those students have only an eighth-grade-level education. I know it's anecdotal, but don't tell me that our education system isn't in trouble. There's currently a furor over the PISA (Programme for International Student Assessment), which evaluates 15-year-olds worldwide. Among the 65 countries that participated in the study, the United States ranked 15th in reading, 23rd in science, and 31st in math. So, although I grew up on dreams of space travel, moon landings, and the engineers who got us there, I'm now more concerned about projects here on earth.

A few months ago, I gave the *Electronic Products* product-of-the-year award to an engineer from Texas Instruments who invented an IC that could help in the design of mobile medical devices. When I spoke with him, I could almost hear the emotion in his voice when he discussed how mobile electrocardiograms in villages throughout India and elsewhere could benefit from his product. And, in Silicon Valley, I recently heard about students who banded together to build robotic legs for a fellow student who had lost his own.

I see Japan calling for the move away from nuclear power—without a substitute to fill its energy needs. And the same scenario applies to the United States: Is nuclear fusion even an option? Can it be a goal? Is it worth pursuing? Some say it is, within magnetically controlled million-degree-Celsius containment fields, but I wonder. Is it still a pipe dream? But so was the moon, at one time.

So, with all that's going on with the economy and all that ails us here on earth, how would you split $10 of your R&D money? Would you put manned space at the top or the bottom of a list that includes education, energy, medical, and military? What would you add to the list? I believe that the shuttle program has run its course, though I'm all for unmanned space exploration. It's a lot cheaper and keeps us in the game, but it would go at the bottom of the preceding list.

This issue is contentious, and I'm probably going to get a lot of flak, but seriously, what do you think should be our next "moon shot"? I can think of many others, besides landing on the next rock. EDN

REFERENCES

1 Pravica, Michael, "The Last Shuttle: A Paean to Spaceflight," *The New York Times*, July 13, 2011, http://nyti.ms/pNniBf.

2 Paletta, Damian; Carol E Lee; and Matt Philips, "Raters put U.S. on Notice," *The Wall Street Journal*, July 9, 2011, pg 1.

Contact me at patrick.mannion@ubm.com.

EDN

pulse

INNOVATIONS & INNOVATORS

IMU provides high accuracy in a compact package

IMUs (inertial-measurement units) provide as much as 6° of freedom, allowing them to measure motion in three dimensions. The consumer-electronics market was until recently the primary driver for advances in IMU technology because the devices find use in handheld game controllers and smartphones. Components for this market have cost and size constraints, so IMUs are typically tiny and low-priced. However, the devices also find use in applications such as industrial control, which have more demanding requirements for accuracy and performance. Targeting this market, Epson Electronics America has introduced the S4E5A0A0 IMU, which measures 6°/hour of gyro bias instability and 0.24°/$\sqrt{\text{hour}}$ of angular random walk.

Employing the company's quartz-based QMEMS (quartz-micro-electromechanical-system)-sensor technology, the IMU is approximately 100 times more accurate than the low-cost IMU technologies that consumer products use, according to Epson. The IMU has a ±300°/sec triaxis gyroscope and a ±3g triaxis accelerometer with an estimated current consumption of 30 mA and a power consumption of 100 mW when operating at 3.3V. It uses an industry-standard SPI (serial-peripheral interface) and a UART (universal asynchronous-receiver/transmitter) interface, measures 24×24×10 mm, and has an operating temperature range of –20 to +70°C. Epson certifies the factory calibrations of the quartz sensors in each IMU that leaves its factories. Sample pricing is $2500 each. **—by Margery Conner**

▷**Epson Electronics America**, www.eea.epson.com.

The S4E5A0A0 IMU measures 6°/hour of gyro bias instability and 0.24°/$\sqrt{\text{hour}}$ of angular random walk to provide motion sensing for applications requiring high accuracy.

TALKBACK

"I've joked for years that, with GPS and portable printers, we could eliminate the police and have the car print the ticket. My 17-year-old then noted that some people would be driving around with so many tickets in the car that they couldn't safely see out the windshield! Technology is great, but we need to be levelheaded about how we apply it."

—Engineering manager Dale Whitworth, in *EDN*'s Talkback section, at http://bit.ly/pbDtNQ. Add your comments.

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Dual-core microcontroller enables "green" designs

To help designers tackle the problem of greater power efficiency, Texas Instruments has announced the C2000 Concerto F28M35x dual-core-microcontroller series, which combines the company's C28x core and control peripherals with an ARM Cortex-M3 core and connectivity peripherals. Together with the company's controlSuite software, the new single-chip C2000 32-bit Concerto series supports real-time control and advanced connectivity in a 144-pin QFP with a starting price of $7.79 (10,000) each.

The benefits of improved power efficiency are clear, particularly in the context of motor control and data centers, with manufacturers shipping 10 billion motors every year and "Googleplex"-like server farms consuming power in the gigawatts sprouting up globally. Every percentage gain in efficiency translates into many saved gigawatts and dollars.

However, according to Keith Ogboenyiya, general manager of TI's microcontroller platform, people talk about the issue solely with respect to power-conversion efficiency. Instead, he says, it's now about making devices intelligent through connectivity: Real-time control requires real-time processing. Still, connectivity has been a bit of a struggle with operating systems and connectivity in a real-time domain.

TI delved into connectivity when it announced the F28x microcontroller line in January. This announcement came with a Viterbi complex-math unit to efficiently execute communications functions, such as those for power-line communications. However, a separate ARM-based device would be a good idea for demanding system control, user-interface, sequencing, monitoring, and host communications.

Yet, opting for two devices brings with it added cost, development, board space, and debugging issues, as well as interprocessor-communication latencies due to the 10-Mbps limitation of the SPI (serial-peripheral-interface) bus.

With these issues in mind, TI has integrated the C28x with the ARM Cortex-M3 to form the F28M35x Concerto. Engineers can tailor performance to their applications with options for 150/75, 100/100, or 60/60 MHz on the C28x and Cortex-M3 cores. As a package deal, the single-chip device reduces complexity, reduces latency to nanoseconds using a shared RAM, and brings advantages in board space and cost.

In a typical application, such as industrial drives and automation, the C28x can handle the variable-speed motor control across multiple motors with precision sensing. Meanwhile, the ARM core takes care of the OS and RTOS; forms the communications bridge, supporting factory-automation protocols, such as Fieldbus, EtherCat, and Profibus; monitors the motion profiles; and provides overall system management.

> It's now about making devices intelligent through connectivity: Real-time control requires real-time processing. Still, connectivity has been a struggle.

In server farms, the division of labor falls along similar lines, with the C28x taking care of power conversion across multiple rails and loads, driving efficient topologies and ensuring power protection, whereas the M3 handles load balancing and diagnostics.

The Concerto platform also comes with interesting safety and security features, some of which are a result of the integration of the two cores. For example, along with two clocks and multiple system watchdogs, the platform provides functional redundancy, whereby one core can check on the other to ensure accurate execution. Two ADCs allow the reliable monitoring of input measurements.

For security, Concerto includes lock protection on GPIO (general-purpose input/output) and registers, memory protection for safeguarding software IP (intellectual property), and the ability to permanently disable JTAG (Joint Test Action Group) for protection against theft. The package also includes error correction and cyclic redundancy checking.

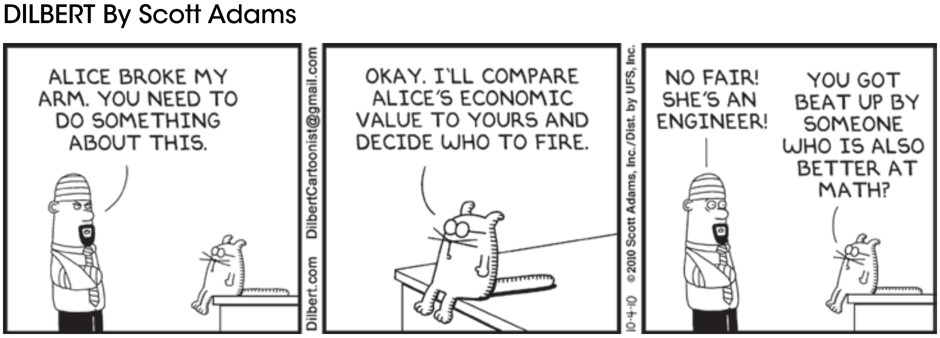
TI promises an intuitive software interface using controlSuite with updated application and communication libraries, with free turnkey application and connectivity-software libraries, including Ethernet and USB (Universal Serial Bus). Digital power, motor control, and renewable energy libraries will be available in the third quarter of this year. According to Ogboenyiya, those energy libraries will include solar, with MPPT (maximum power-point tracking), dc/dc, and dc/ac.

The device is available for sampling. TI provides a $139 Concerto experimenter kit, with a $99 controlCard and docking station. An overview of the platform is available at http://bit.ly/iMf0d5.

—by Patrick Mannion

▷**Texas Instruments**, www.ti.com.

DILBERT By Scott Adams



RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Looking for savings in all the wrong places

Q. I'm trying to save cost and printed-circuit board space. Can I use an amplifier's internal ESD diodes as clamping diodes?

A. In this design, the input signal periodically went above the supply voltage, so this customer wanted to use the amplifier's internal ESD diodes to clamp the signal. While this sounds like a good idea, it's really not. Like anyone, the designer wanted to save money and PCB area, but he was looking in the wrong place to save. In the end, his solution would end up costing him more time and money, as he'd have to keep replacing amplifiers that acted like fuses.

Why is that? In our amplifiers, ESD diodes are connected between the input and output terminals and the supply terminals. The ESD diodes protect the amplifier by routing energy from an ESD event away from the amplifier and to the supply rails. ESD diodes are only designed to operate for short periods of time. Running them continuously could damage or destroy the diode, or the bond wires, or the amplifier itself. Even if the amplifier wasn't destroyed, excessive heat generated due to sustained operation of the ESD diodes could degrade the amplifier performance, which could cause latent defects.

A second problem with using the internal ESD diodes as clamps is that the inputs of the amplifier would have to go above the supply rails for the diodes to conduct. This would exceed the Absolute Maximum Ratings for the amplifier's input voltage. This is another no-no, as discussed in RAQ #50, "What's the big deal about ABSOLUTE MAXIMUM RATINGS?" Stay away from Absolute Maximum Ratings; nothing good can come from operating near them, even for just a little while.

A better way to protect the amplifier is to use a set of external diodes, with a current limiting resistor tied to a lower supply voltage than the recommended maximum input voltage of the amplifier.

Another option, fairly new to the market, is to use an amplifier with built in Overvoltage Protection (OVP). Analog Devices offers several amplifiers with OVP, including the ADA4091-2, ADA4092-4, and ADA4096-2. In the long run, these options provide a safer, more cost effective solution to protecting the amplifier and downstream circuitry.

To Learn More About Input Protection
http://dn.hotims.com/34938-100

Contributing Writer John Ardizzoni is a Senior Application Engineer at Analog Devices in the High Speed Linear group. John joined Analog Devices in 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 30 years experience in the electronics industry.

Have a question involving a perplexing or unusual analog problem? Submit your question to: www.analog.com/askjohn

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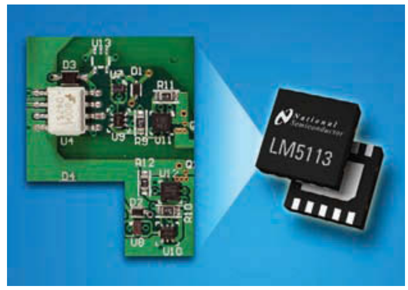
Industry's first eGaN-FET driver simplifies switching design

As switching devices for high-voltage power-conversion circuits, GaN (gallium-nitride) FETs appear poised to eat into silicon FETs' market share. GaN-FET technology has a lot going for it. For example, the FETs boast a lower on-resistance than competing units, resulting in lower switching loss, a lower gate charge, and, in turn, faster switching. They also have much smaller footprints than do silicon devices.

Conventionally, a GaN device operates in depletion mode, meaning it is normally on: When you initially apply power, the GaN FET is in its on state—the opposite of silicon FETs. This situation is potentially hazardous.

To address this problem, EPC (Efficient Power Conversion, www.epc-co.com) manufactures eGAN (enhancement-mode-GaN) FETs. EGaN FETs behave in a similar way to MOSFETs, use a bulk-CMOS process, and can take advantage of the inherent advantages of the process. The technology poses some design challenges for gate drivers, however. For example, they are more sensitive to gate overstress than are MOSFETs; their absolute gate voltage must be less than 6V, and their gate-threshold voltage, at less than 1.4V, is much lower than that of MOSFETs. They are also prone to fault turn-on due to dV/dt (change in voltage over time) during turn-off, and they require a low-impedance driver for turn-off.



This 180W, one-eighth-brick, fully regulated converter demonstrates the system-performance advantages of coupling eGaN FETs with the LM5113 driver (courtesy National Semiconductor).

To counter these challenges, National Semiconductor recently introduced what it claims is the industry's first 100V half-bridge gate driver for use with eGaN FETs in high-voltage power converters. The new LM5113 high-side and low-side GaN-FET driver reduces component count by 75% and uses as much as 85% less PCB (printed-circuit-board) area than discrete-driver designs.

According to the company, the device uses proprietary technology to regulate the high-side floating bootstrap-capacitor voltage at approximately 5.25V to drive eGaN power FETs without exceeding the maximum gate-source voltage rating. The LM5113 also features independent sink and source outputs for flexible turn-on strength with respect to the turn-off strength.

A 0.5Ω-impedance pulldown path provides a fast, reliable turn-off mechanism for the low-threshold-voltage eGaN power FETs. The LM5113 also integrates a high-side bootstrap diode, further minimizing PCB real estate, and provides independent logic inputs for the high- and low-side drivers, enabling flexibility for use in a variety of both isolated- and nonisolated-power-supply topologies.

The LM5113 comes in a 10-pin 4×4-mm LLP and costs $1.65 (1000).

—by Margery Conner

▷**National Semiconductor**, www.national.com.

Microcontrollers add FPU, raise flash support

Freescale Semiconductor's seventh Kinetis microcontroller family employs the ARM Cortex-M4 core. The Kinetis K70 family will include an FPU (floating-point unit), tamper detection, graphics-LCD capabilities, and as much as 1 Mbyte of flash memory. Freescale introduced the Kinetis platform in 2010, and it now contains a portfolio of pin-, peripheral-, and software-compatible devices. The portfolio includes HMI (human-to-machine-interface), connectivity, safety, and security peripherals.

In the fourth quarter of this year, Freescale plans to introduce additional devices in the Kinetis K10, K20, and K60 families, which also have single-precision FPUs. These devices will extend the range of data-acquisition-intensive applications, such as brushless-dc motor control and digital filtering, by reducing computation time and code size and increasing system accuracy.

They will include high-speed USB (Universal Serial Bus) host/device/OTG (On-the-Go) functions supporting 480-Mbps data transfer using an external ULPI (USB 2.0-transceiver-macrocell-interface low-pin-interface) transceiver and hardware-tamper-detection-unit-integrated sensors for voltage, frequency, temperature variation, and detection of physical attack.

DRAM and NAND-flash controllers will enable the connection of DDR, DDR2, and low-power DDR memories, along with as much as 32 bits of ECC (error-correcting-code) NAND memories. The graphics LCD, which is only on the Kinetis K70 family, supports QVGA (quarter-video-graphics-array) LCD panels as a single chip and as much as 24-bit SVGA (super-VGA) panels using external memory, which Freescale's PEG (portable embedded-graphical-user-interface) library supports with a simple WindowBuilder interface for GUI (graphical-user-interface) development.

The device will include an analog-signal-measurement and -conditioning engine to provide single-chip processing capability for portable medical, instrumentation, and test-and-measurement applications. USB, Ethernet, segment-LCD, and encryption modules provide options for secure data transmission between system components and the end user through a display.—by Colin Holland

▶**Freescale Semiconductor**, www.freescale.com.

07.28.11


Name
Dr. Christian Altenbach, Certified LabVIEW Associate Developer
Job Title
Research Ophthalmologist
Area of Expertise
Biophysics
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Mapping molecular structure changes during activation of the light receptor, rhodopsin
NI LabVIEW
LabVIEW makes me better because I can
PROGRAM
the way I think

Rohde & Schwarz, Synopsys team up on LTE

Rohde & Schwarz and Synopsys have announced a collaborative effort to accelerate LTE (long-term-evolution) and LTE-Advanced wireless-system design and verification. Synopsys is contributing its algorithm design and verification tools, including standards-compliant reference libraries. Rohde & Schwarz is contributing its SMU200A and SMBV100A vector-signal generators, against which it has verified the Synopsys LTE and LTE-Advanced libraries to increase designer confidence in achieving standards compliance when evaluating prototypes and samples. Synopsys' LTE library for its System Studio and SPW (signal-processing-workstation) algorithm design products includes models of the transmitter and the physical channel that the standard defines as well as functional models of ideal receivers that can serve as references. The library provides an end-to-end simulation chain for both uplink and downlink transmission and reception.

The companies will verify Synopsys' upcoming LTE-Advanced enhancements against the Rohde & Schwarz signal generators, which in turn will be able to automatically derive their configuration from the Synopsys simulation setup. Because typical configurations comprise more than 100 parameters, this integration reduces the time it takes to achieve a correct setup. The integration also reduces the risk of configuration inconsistencies that often result in losing days of system-integration time in the lab.

According to Markus Willems, senior product-marketing manager for system-level products at Synopsys, and Simon Ache, product manager for signal generators and power meters at Rohde & Schwarz, Rohde & Schwarz and Synopsys found that they were talking to many of the same companies but to different teams within those companies when marketing LTE-related offerings. Whereas Synopsys was addressing concept engineers and algorithm designers, Rohde & Schwarz was addressing manufacturing engineers and chip-set developers working with real silicon. Rohde & Schwarz and Synopsys then realized they could collaborate on assisting both the algorithm designers and the chip-set developers.

> "The companies could assist both the algorithm designers and the chip-set developers.

The ability to validate an LTE library against a signal generator enables I/Q (in-phase/quadrature) signal equivalence for both algorithm designers and chip-set developers. The use of a bit-equivalent I/Q signal throughout all phases of the design—from concept to final hardware test—facilitates comparison and cross-analysis throughout the process and increases confidence in standards compliance. In addition, it simplifies debugging should an inconsistency occur between simulation and hardware test. From an instrument perspective, the SPW/System Studio automatic-configuration capability speeds test-equipment setup and avoids the loss of system-integration time because of configuration errors. It also ensures consistency of signal generation for both simulation and test, and it supports the reuse of regression scripts from simulation setup during integration testing.

The validated Synopsys LTE library will become available with the 2011.06 release, which will also include the initial version of LTE-Advanced. Access is free to all Synopsys LTE-library customers who have maintenance contracts. The LTE library works for both SPW and System Studio. The automatic configuration of Rohde & Schwarz signal generators from Synopsys' algorithm-simulation tools, SPW, and System Studio, will be available in October.

—by Rick Nelson

▷**Rohde & Schwarz**, www.rohde-schwarz.com.

▷**Synopsys**, www.synopsys.com.

Veredus uses STMicro's Lab on Chip to detect food-borne pathogens in less than two hours

The recent E Coli (Escherichia Coli) outbreak in Germany resulted in the deaths of more than 30 people and the hospitalization of many more. The German government took a lot of criticism for its apparent fumbling of the investigation into the source of the contamination. Government-response time aside, tracking down biological contaminants is not simple: Lab tests on genetic information on the source of an infection can take days to weeks to perform.

Given those facts, Veredus Laboratories (www.veredus labs.com) has made a timely introduction: VereFoodborne, a device that can detect 10 to 12 food-borne pathogens, including the Shiga-toxin-producing E Coli, salmonella, listeria, and campylobacter, in one test. It returns results within two hours rather than days.

The VereFoodborne can detect 10 to 12 food-borne pathogens in one test that takes two hours (courtesy Veredus Laboratories).

Veredus based the product on STMicro's Lab on Chip platform, which comprises a microarray on the chip that allows it to detect multiple pathogens in one test. The chip sells for $100 to $150.

—by Margery Conner

▷**STMicroelectronics**, www.st.com.


Name
Hector Guajardo Betancourt, Certified LabVIEW Architect
Job Title
Automated Test and Control Engineer
Area of Expertise
Manufacturing Test
LabVIEW Helped Me
Reduce test time by more than 10X
Latest Project
Building a vision-based inspection system for washing machine drums
NI LabVIEW
LabVIEW makes me better because I can deliver multiple
PROJECTS
on time, on spec, and on budget

VOICES

Avnet's Alex Iuorio: Micro issues in the electronics supply chain are no small matters

Alex Iuorio, senior vice president, supplier management, at Avnet Electronics Marketing Americas, spoke with *EDN* at the end of June as many companies were preparing for their second-quarter statements. From his viewpoint, as an expert on the electronics supply chain, Iuorio addressed statements on bookings, component demand, and expectations for the year. An excerpt of that discussion follows.

In late June, financial reports and company guidance began noting softening bookings. What are your thoughts?

A As we think about that and home in on it [regarding] the electronics industry ... there seem to be some plausible reasons for it. If you start with the [earthquake and tsunami in March] in Japan, clearly what that did was take what would have been June-quarter bookings and move them into the March quarter to some percentage.

The second factor is that we're coming off the 2008/2009 recession and the subsequent bounce back, which in the high-tech world looked like a straight-up V, and that [situation] extended lead times. That [scenario] went on for a while, and then kind of slowed down.

And the third factor is clearly the summer slowdown: a cyclical slowdown in the United States and Europe that has been there forever.

When you factor in those things and you look at the overall softness of bookings, it seems pretty reasonable that we would be where we are.

If you put all those factors together with the fact that customers seem to be chugging along at normal tolerances, it would seem that this [situation] is an inventory correction of sorts and not really a comment on underlying demand. There are a lot of people talking about softened bookings, but nobody seems to be talking about the reasons [for them]. We immediately revert to the macro issues and we are sensitive to those issues, but micro issues for our industry prevail here.

Gartner in June lowered its estimate for 2011 semiconductor revenue to around 5.1% growth, down from an earlier 6.2% estimate. However, IHS iSuppli in June raised its estimate for 2011 semiconductor revenue to 7.2% growth from the 7% projection it made earlier. What do you think of those figures?

A If you [can agree] that there is an inventory correction in the industry, then

you [can agree] that our information systems as an industry are strong enough to react both upside and downside so it doesn't get too far out of control. The carry-through would be that we'll burn it off in 60 or 90 days, and we will still have enough time to be able to catch those forecasts. Somewhere between Gartner and IHS iSuppli is going to be reality for the year.

Are you happy with that situation?

A In some respects, the western world has matured, and mature industries tend to grow at those kinds of rates. I'm just happy that the forecast looks to be legitimate and that the industry is showing that type of growth.

Where is engineers' design demand coming from?

A We've established a lighting business to address high-brightness-illumination applications within our standard customer base but also to address the lighting industry itself—these luminaire manufacturers that are going toward high-brightness technologies and need processor control, the thermal solutions, optics. The lighting industry is a great metaphor for what we see. More and more, our daily life is becoming processor control. [An analyst company in June] revised estimates [upward] for electronics in the automotive market. Cars were already chock-full of components and were processor-controlled, so we are talking about an increase in electronic content. Aerospace/defense also continues to grow. That market is an interesting one because all that defense spending is stable at best, probably declining. However, electronics content within government systems continues to grow. Beyond that, medical electronics is a growth area. But the general answer is that it's really about everything becoming more dependent on processor control, and, when you are more dependent on processor control, you're talking directly about microprocessors and microcontrollers. [That scenario] will help drive us.

Are you seeing more demand for the design-chain parts of Avnet's business?

A Today, we really think of the design chain and the supply chain as linked. But everybody is playing for bigger chips. You have to be able to design in the right products, and the right product has to be designed as not only the right fit, form, and function for the application but also producible and available at the time the customer wants to hit its market window. In short, we are seeing a lot more consultative use of our design teams, our FAEs [field-application engineers], and our business-development managers in helping customers decide what the right [technology] is so that it fits the application so that it's available when they want it.

—interview conducted and edited by Suzanne Deffree

BY BONNIE BAKER

Use an RC filter to "deglitch" a DAC

Annoying speed bumps, which have become ubiquitous on roadways, force you to either slow down or find a way around them. While driving recently, I needed to negotiate one of those bumps, and doing so reminded me of a precision, 16-bit DAC using an R2R architecture, which places resistors in parallel as a resistor ladder (**Figure 1**). The DAC had a glitch at midscale. You can add deglitching circuits to DACs such as these ones that share traits with speed bumps: To avoid them, you must either slow down or find a way around them. Two common DAC-deglitching circuits accomplish these tasks. Simple lowpass filters represent a slowdown tactic, and sample/hold circuits offer a way to avoid the glitch. These deglitching circuits can either decrease the glitch's amplitude or remove its energy.

The simplest DAC-deglitching method uses an RC filter (**Figure 2a**) at the DAC's amplifier output, V_{OUT}. This filter attenuates the amplitude of the glitch and increases the settling time. In **Figure 2b**, the top curve (red) is the signal on the DAC's LDAC (load-DAC) pin. You serially load a data word into the DAC using the DIN (data-in) and clock (CLK) pins. Once the DAC has a complete word of data, the rising edge of the LDAC pin loads the data word into the internal DAC registers. This action initiates a change in the DAC's output voltage. The middle curve (yellow) shows the measured midscale analog glitch from the DAC's output. The bottom curve (green) shows the measured analog signal after an RC lowpass filter.

When you increase or decrease the data-code value, the output voltage also increases or decreases. But at midscale, one-fourth scale, and three-fourths scale, the DAC generates a glitch—the midscale glitch being the largest. To determine the appropriate RC ratio, examine the glitch period and select a 3-dB point for your filter approximately one decade lower than the glitch frequency.

For example, the glitch period in **Figure 2b** is approximately 1 μsec. This value translates to a 1-MHz glitch period. From this estimate, the RC values in **Figure 2** create an 80-kHz lowpass filter. When selecting your RC values, make sure that the resistance is low enough to avoid loading errors. This RC filter solves the R2R DAC-glitch problem, but there is no free lunch. As you can see from the bottom curve in **Figure 2b**, the RC filter extends the DAC's settling-time output signal.

Depending on your application's requirements, a simple RC filter may do the trick. If the system calls for an R2R DAC that has an interfering glitch, you might be able to combine a switching capacitor with an RC filter to solve the problem. EDN

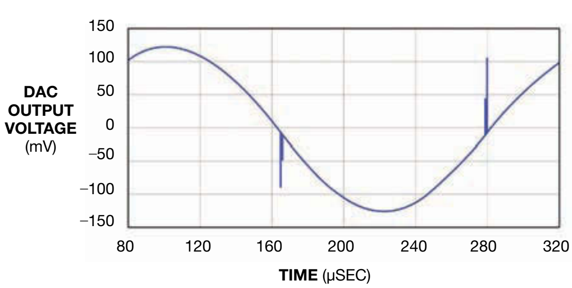

Figure 1 You can use an R2R architecture, which places resistors in parallel as a resistor ladder, to deglitch a DAC.

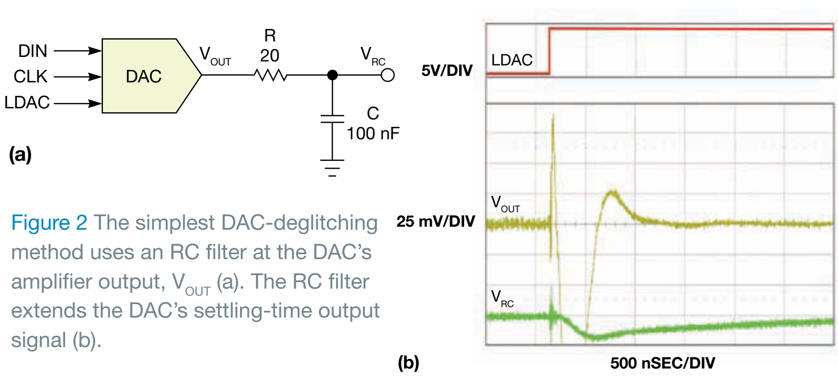

Figure 2 The simplest DAC-deglitching method uses an RC filter at the DAC's amplifier output, V_{OUT} (a). The RC filter extends the DAC's settling-time output signal (b).

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ACKNOWLEDGMENT

The author wishes to give special thanks to Tony Calabria, a precision-analog-applications engineer at Texas Instruments.

Bonnie Baker is a senior applications engineer at Texas Instruments.


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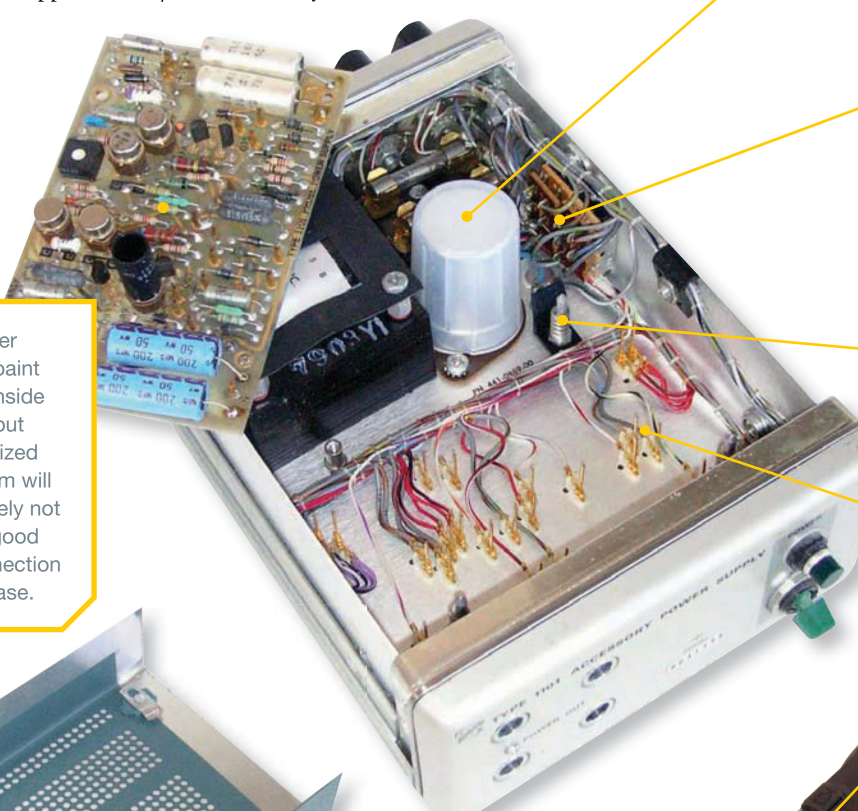
The Tektronix 1101 oscilloscope-probe power supply

When Tektronix created its line of powered FET oscilloscope probes, it needed a way to supply power to them. In 1969, the company developed the 1101 accessory power supply. The unit can power four probes. It supplies ±15V, 5V, and chassis common to the four front-panel connectors. The metal chassis connects to earth ground, as the law requires. This linear power supply has three TO-66 pass transistors. A switching supply would add noise to the probes it powers. The circuit has 10 single transistors and three matched transistor pairs. The circuit sequences the power and shuts down if any supply fails. The PCB (printed-circuit board) has neither pigtails nor edge-card connectors, which tend to fail under vibration. Instead, Tek engineers designed a delicate and complex system of pins that engage sockets soldered into the PCB. Spring-loaded snaps in three places retain the circuit card. A screw in the fourth corner ensures a secure connection to chassis common. This approach is an expensive design expedient, but a simpler approach may have worked just as well.

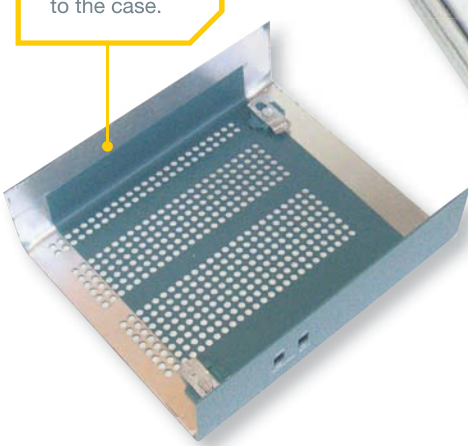


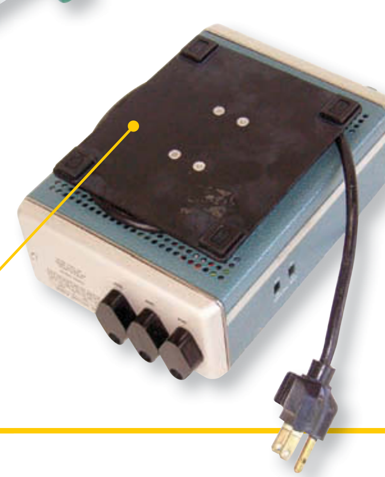
C41 is a 1000-μF capacitor for the 15V supply. The case floats at a negative potential, so Tek engineers covered it with a plastic housing.

Switches on the side let you set the supply for 110 or 220V input power and the high and low line voltage.

The PCB pops out once you remove the grounding screw and push three plastic catches. Less attractive are the 22 delicate gold-plated pins that must align perfectly to engage sockets in the PCB.

The cover has no paint on the inside edges, but the oxidized aluminum will most likely not form a good RF connection to the case.





A Tek system-level designer realized that dangling power cords bedevil engineers, so he added this handy cord caddy to the bottom of the unit.

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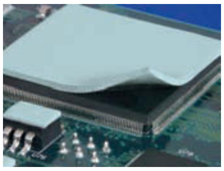

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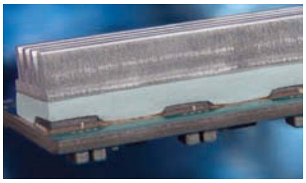

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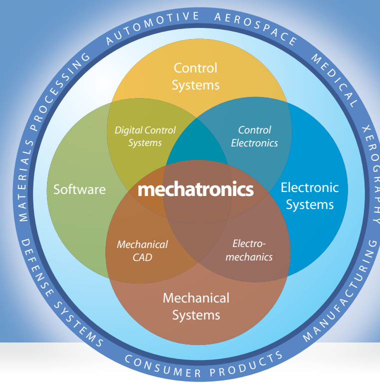

Improving mechatronic-system design

A model-based approach takes your design from concept to working system.

By Kevin C Craig, PhD

The top drivers in industry today for improving development processes are shorter product-development schedules and increased customer demand for better-performing products. As engineering systems become more multidisciplinary and complex, can you simultaneously achieve these two goals?

Challenges inhibiting mechatronic-product development involve the multidomain nature of the complete system, the integration of the domains, and the discovery of errors early in the development cycle and testing before hardware is available. Once a system is in development, correcting a problem costs 10 times as much as fixing the same problem in concept. If the vendor has released the system, it costs 100 times as much.

An innovative approach to mechatronic-system design addresses these challenges. Through system modeling and simulation, it facilitates understanding the behavior of the proposed system concept by optimizing the system-design parameters, developing local and supervisory control algorithms, testing control algorithms under various scenarios, and qualifying the production controller with a simulated version of the plant running in real time before connecting it to the real plant (**Figure 1**).

The process provides an environment that is rich with numerical- and graphical-analysis and design tools that stimulate innovation and cooperation within design teams. It aims to reduce the risk of failure to meet the functional requirements by enabling early and continuous verification throughout the entire design workflow. EDN

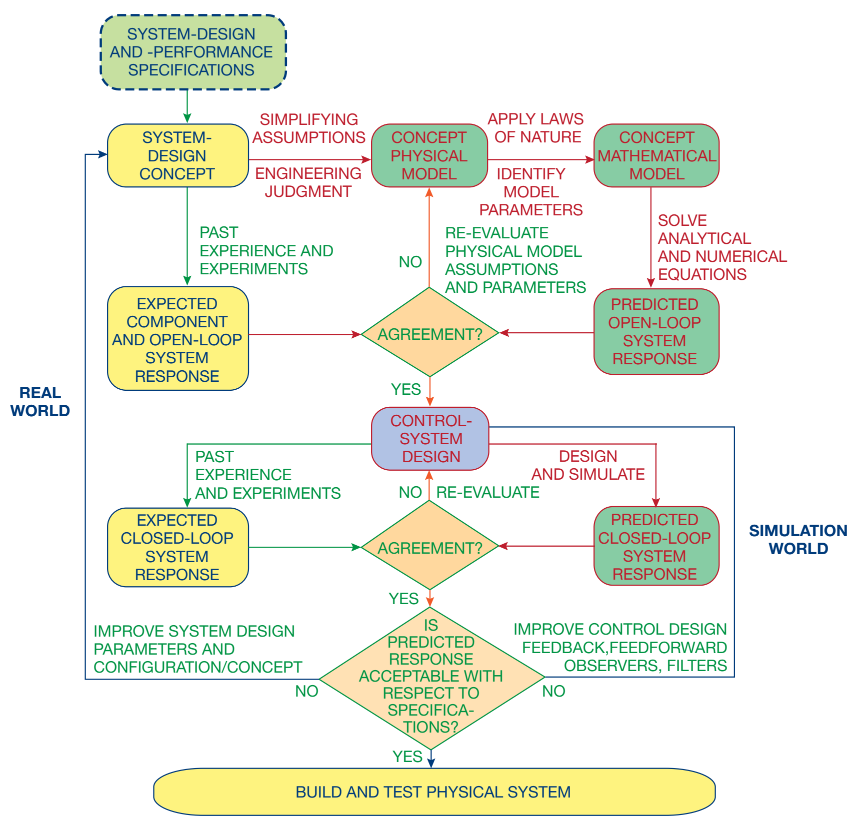

Figure 1 An innovative approach to mechatronic-system design facilitates understanding the behavior of the proposed system concept by optimizing the system-design parameters, developing local and supervisory control algorithms, testing control algorithms under various scenarios, and qualifying the production controller with a simulated version of the plant running in real time before connecting it to the real plant.

IC-LIKE MODULES **SIMPLIFY** SYSTEM DC/DC **POWER DESIGN**

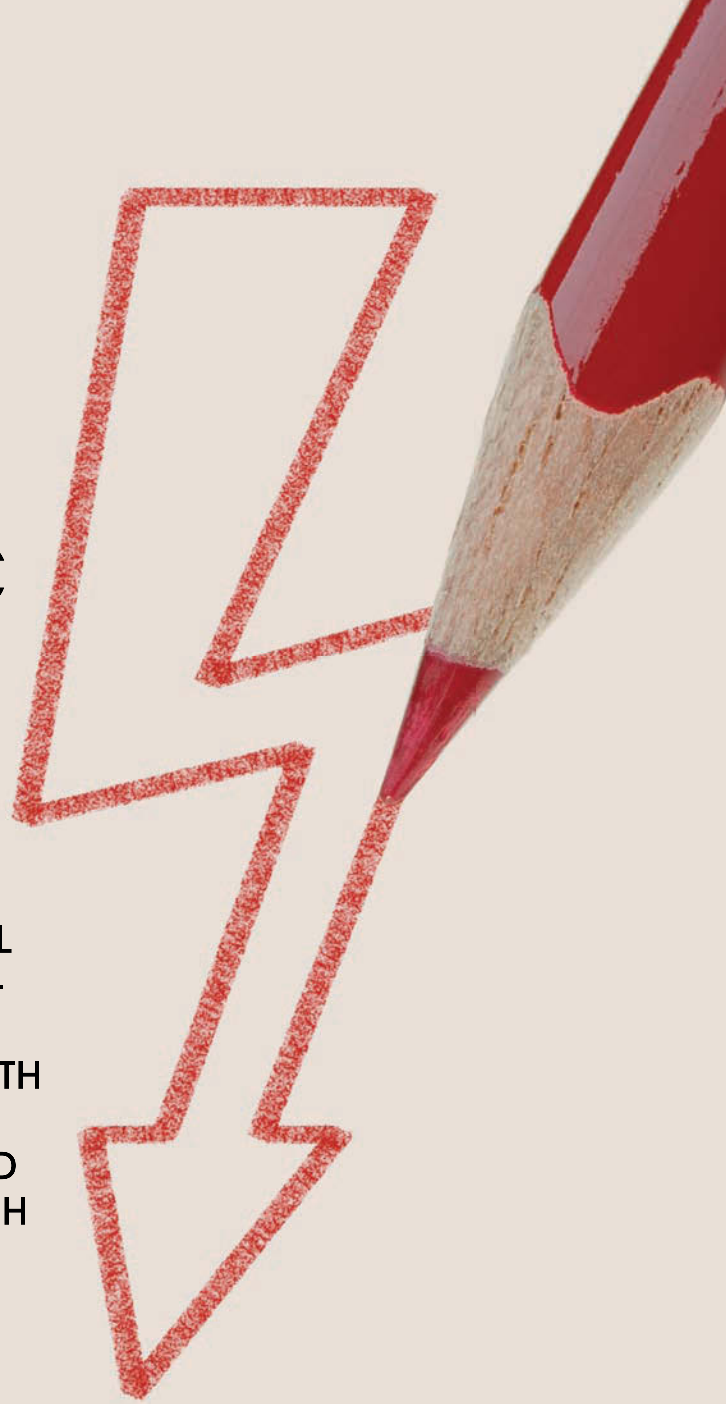

IMAGE: ISTOCK

POWER MODULES ENCAPSULATE POL POWER-MANAGEMENT AND POWER-CONVERSION DEVICES, INCLUDING INDUCTORS, INTO ONE PACKAGE WITH THE LOOK AND FEEL OF AN IC. THEIR PREDEFINED LAYOUTS AND MATCHED COMPONENT SELECTION MEAN HIGH POWER DENSITY, LOW NOISE, AND RELIABLE PERFORMANCE.

BY MARGERY CONNER • TECHNICAL EDITOR

Power-management designers and system architects struggle to meet the increasingly tight performance demands of load ICs, such as FPGAs, DSPs, and CPUs. To meet higher processor-clock frequencies, these power-hungry ICs require voltages of less than 1V, resulting in falling POL (point-of-load) voltages and rising currents. In addition, they require tighter voltage-setpoint windows, lower output-voltage ripple, faster transient response, and reduced noise generation. Even as the design constraints grow tighter, design time shrinks because developers often define the power budget and PCB (printed-circuit-board) space for power chores at the end of the specification cycle.

An approach that is gaining momentum for nonisolated POL power-management designs is the use of a module to encapsulate the power semiconductors and ICs in unpackaged dice, along with passive devices, including the inductor, in the same form factor as an IC. Because magnetics do not comply with Moore's Law, the inductor takes up most of the component space (**Figure 1**). Applications for modules typically align with current requirements. Modules with currents of 4A and lower fit portable devices, whereas devices that provide current as high as 10 or 12A fit into stationary equipment.

The PSMA (Power Sources Manufacturers Association) has defined an encapsulated power supply with an integrated discrete inductor within the package as a PSIP (power supply in package). The term has some traction in the power-design community, but the industry more typically uses the term "module." The PSMA draws a distinction between PSIPs, which have a discrete inductor within the module, and a power SOC (system on chip), in which the silicon inductor is either discrete or integral to the IC (**Reference 1**).

Power modules have several advantages over discrete power designs. For example, PWM (pulse-width-modulated) power converters operate at hundreds of kilohertz, so both radiated and received converter noise can be a concern, necessitating the shortest possible signal traces. Modules also include an inductor and capacitors that match the overall design and switching frequency and can include 3-D assembly of components, a task that is beyond the reach of a simple PCB-mounted discrete power implementation. Further, modules' IC form factors suit pick-and-place assembly, and the modules have passed noise certification from standards bodies such as CISPR (Comité International Spécial des Perturbations Radioélectriques) 22, Class B, for radiated and conducted EMI (electromagnetic interference). This compliance guarantees that the ubiquitous bugaboo of noise will not be a concern for designers.

AT A GLANCE

- A power module encapsulates the power semiconductors, control circuitry, and inductor into a module with the form factor of an IC.
- Using a module allows you to outsource the POL (point-of-load) power subsystem's design and manufacturing.
- High power density and low noise result from internal 3-D assembly in the module.

Power modules are not inexpensive alternatives to designs using off-the-shelf discrete devices. Given their advantages, however, they can be cost-effective and allow designers to outsource their power-design chores. Keep in mind that these modules do not encompass open-frame power regulators, in which the components mount on a PCB—usually some form of FR-4 (flame-retardant) material—and are left open. DOSA (Distributed-Power Open Standards Alliance) covers these types of regulators (**Reference 2**).

Although modules can go a long way toward solving noise-related packaging problems, thermal issues still remain. In addition to enhancing the "green" quality of an end product, a more efficient power module means less wasted power and thus has less heat to dissipate. After power-conversion efficiency, the most important thermal specification for your design is the thermal resistance of the module. Check that the $\theta_{J/A}$ (thermal resistance from the semiconductor junction to the ambient air) allows adequate heat dissipation. If not, you must trade off space by adding a heat sink or a fan.

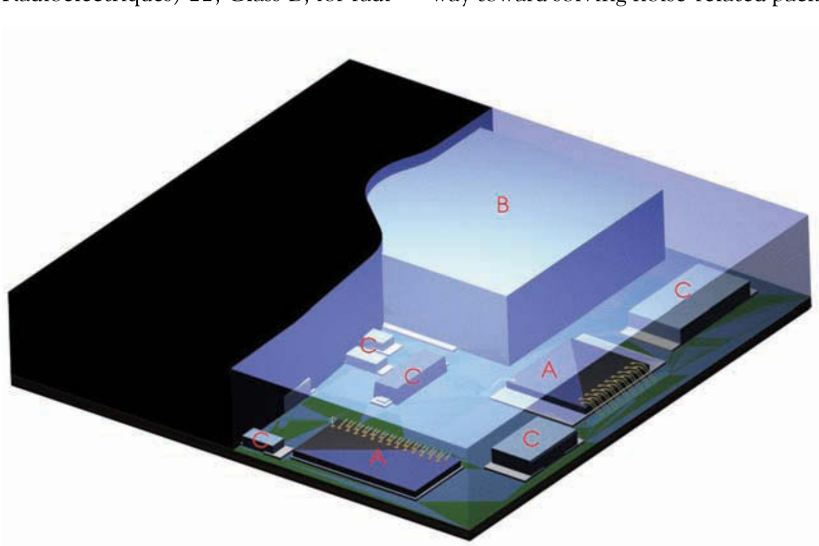

Figure 1 Power modules, or PSIPs, encapsulate the power-conversion and control silicon along with the power inductor and other passives; the power inductor dominates the module space. The parts labeled A indicate Linear Technology silicon; B indicates magnetics; and C indicates capacitors, resistors, and diodes.

Clever packaging is behind most modules' increasing power density. An example of increasing density through packaging advancements is National Semiconductor's LMZ series of power modules, which the company introduced in early 2010. In their initial version, the modules were available in a seven-lead, 10.16×13.77×4.57-mm package and supported the common 3.3, 5, 12, and 24V input-voltage rails and load currents as high as 4A at an output voltage of 0.8 to 5V. Prices ranged from $7.10 to $9.50 (1000). The company has since introduced new members of the LMZ family in the same seven-lead package. The new devices drive as much as 5A of output current; modules that provide 8 and 10A come in an 11-pin, 15×17.8×5.9-mm package and sell for $10.93 to $18 (**Figure 2**). You can parallel the higher-current parts for designs requiring higher-than-10A current. Paralleling and synchronization have become standard features of almost all vendors' high-current modules.

POWER MODULES ALLOW DESIGNERS TO OUTSOURCE THEIR POWER-DESIGN CHORES.

Enpirion offers the EN63A0QI module, a member of the EN6300 family, which accepts 2.375 to 6.6V input and provides continuous output current as high as 12A in a 10×11-mm package. The company also offers the EC2630 intermediate-bus converter as a front end for these devices in 12V-rail applications. Enpirion's current silicon process tops out at a 6.6V input. However, according

Figure 2 National's LMZ22010 power module accepts an input-voltage range of 6 to 20V, delivers an adjustable output voltage of 0.8 to 6V, drives as much as 10A of output current, and includes frequency synchronization and current sharing.

to Ashraf Lotfi, Enpirion's chief executive officer, the company plans to move to a 12V process for future products.

A move to higher frequencies is module manufacturers' most straightforward path to shrinking inductors. The EN6300 family, for example, has switching speeds in the megahertz range, which makes the inductor small enough to become part of the module's lead frame (**Figure 3**). "For higher power levels, integrating the inductor into the lead frame allows us to leverage the 200-micron thickness of the lead frame to keep the resistance down and support higher current levels," says Doug Lopata, vice president of design engineering at the company.

Enpirion leads the industry in a move toward a true inductor on silicon; according to Lotfi, the company is making modules with silicon-embedded inductors available for sampling. However, this approach would most likely work only with modules requiring low current.

Virtually all of the vendors in this market claim that inductor design makes up a large portion of their IP (intellectual property). For example, National Semiconductor's modules use a proprietary encapsulant around the inductor itself. The encapsulant is impregnated with iron filings that effectively make it a magnetic shield. Similarly, Vicor's modules switch at frequencies higher than 1 MHz so that they can use smaller magnetics. This approach requires the use of proprietary core materials, according to Philip Davies, vice president for global sales and marketing at the company. Besides concerns about magnetics, ven-

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RELIABILITY: THE OTHER PARAMETER IN DC/DC-REGULATOR SELECTION

By Afshin Odabaee, µModule Power Products

Imagine a complete dc/dc-regulator circuit in a package similar to that of an IC. Let's say that you have examined a selection of products from several vendors and all perform power conversion and meet most of your requirements. How do you determine which one is the best product for your design? You must consider what your customer values from the end product that you create and produce and which dc/dc-regulator parameters define performance. During your selection process, remember the other parameter: reliability. Study the reliability report for each regulator and look for products that have undergone rigorous testing from companies with a reputation for performance and reliability.

Some system designers do not need a high-end and high-reliability dc/dc regulator. These products command a premium that often deters designers from choosing them. Designers sometimes spend time and resources perfecting complex digital sections of a system and are then unaware of how to select the appropriate dc/dc regulator for the design. It is imperative to carefully examine the vendor's reliability-test methods to avoid significant costs later in design alterations and energy on debugging the power management of the board. Verify and compare the reliability data beyond FIT (failure-in-time) rates and superficial numbers. Ask for the details. For those system designers striving to deliver competitive products, choosing a high-end dc/dc regulator that has the backing of a rigorous and systematic reliability-test program ensures good reliability at the system level and a solid reputation for your products with your end customers.

A savvy engineer should study certain parts of a reliability report. First, this report should be available online without the need to request it from the vendor. Second, the vendor must update it at least once a year. A vendor that is transparent with its reliability data is typically spending resources on test equipment, test time, and engineering attention to back its report (Reference A). This report includes tests for operating life; preconditioning; temperature and humidity bias; power cycle; temperature cycle at various temperature ranges; thermal shock at various temperature ranges; solder shock; high-temperature bake at various temperature ranges; mechanical shock; vibration-variable frequency; and board-mount temperature cycle at various temperature ranges.

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Author's biography

Afshin Odabaee is product-marketing manager at µModule Power Products.


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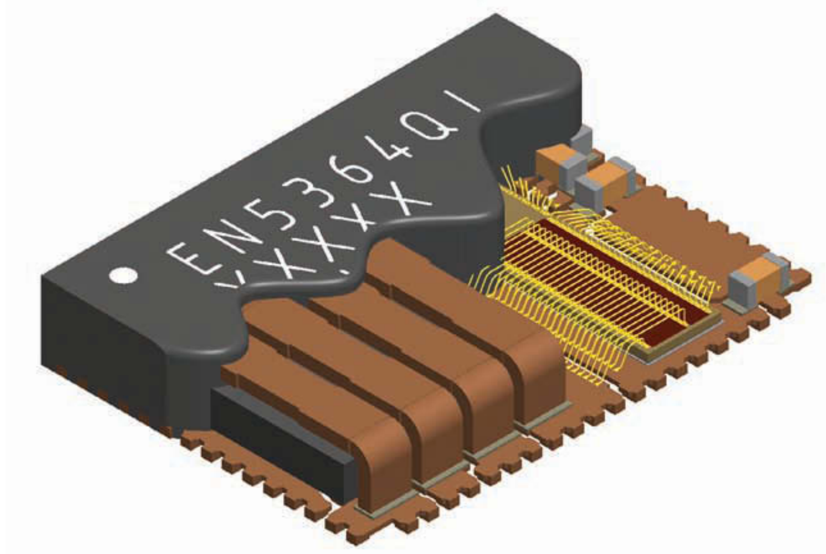

Figure 3 Enpirion's EN5364 power module integrates an inductor directly into the lead frame of the module to conserve space.

dors must carefully select their modules' power ICs, semiconductor packaging, and substrate. Vicor, for example, uses a proprietary derivative of the FR-4 PCB material; Linear Technology uses a BT (bismaleimide-triazine) substrate.

Because of their price premium, power modules fit well in applications that are also in high-end markets, such as banking, data communications, telecommunications, and the military, which place a priority on reliability. Module vendors are also seeing an increase in designs from the automotive industry, in which high quality rankings are important to automakers' success. Space is often at a premium in vehicles. For example, the rear-view mirror, which is part of the automobile's control center, must be unobtrusively small in an electrically noisy environment (see **sidebar** "Reliability: the other parameter in dc/dc-regulator selection").

Most currently available power modules are nonisolated dc/dc converters, and they are subject to the performance pressures of the breed: tighter voltage ranges, lower output-voltage ripple, faster transient response, and reduced noise generation. And, just as in the conventional power-supply- and power-controller-IC world, digital power has a small but interesting role in addressing these challenges. For example, Intersil this year introduced the 15×15-mm ZL9101 digital-power module. The device integrates not only power-conversion components but also power-management features, such as ramp and delay control, sequencing, margining, and tracking; fault-management features, including overvoltage, overcurrent, and overtemperature protection; and telemetry features, such as voltage, current, and temperature monitoring.

The ZL9101M operates over an input-voltage range of 4.5 to 13.2V and supports an output-voltage range of 0.6 to 4V; external resistors or a serial-PMBus (power-management-bus) connection set these ranges. The output current is as high as 12A, and you can precisely regulate the output voltage to as low as 0.6V with ±1% output-voltage regulation over line, load, and temperature variations. It sells for $18.24 (1000).EDN

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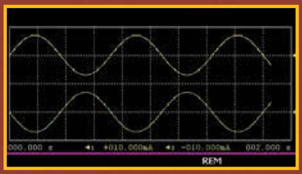

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BY JANINE LOVE • EDITOR, MEMORY DESIGNLINE

As the number of mobile devices worldwide surges, the need for better, cheaper memory for these devices soars. Numerous alternatives are available for mobile memory. Industry standards abound, and others are still in development. By all accounts, this market is on the upswing, so where do all of the memory technologies and form factors fit in, and what's on the horizon for mobile memory?

According to estimates from IHS iSuppli Research, the growth of sales for smartphones and tablets will increase revenue in the mobile-memory market by 26% in 2011 to $16.4 billion, compared with $13 billion in 2010 and, iSuppli projects, $19.3 billion in 2012 (**Reference 1**). Gregory Wong, principal analyst at Forward Insights, agrees that consumer devices, particularly smartphones and tablets, are driving memory demands. He observes two basic types

IMAGE: GORDON STUDER


SAMSUNG

AT A GLANCE

- Mobile devices create a bottomless market for memory ICs.
- Standards, particularly from the JEDEC (Joint Electron Device Council) Solid State Technology Association, are vital to evolution in mobile memory.
- Solid-state drives are starting to change the level of integration for mobile memory, especially in tablets.

of memory available for these devices: *e*•MMC (embedded multimedia card), a low-power JEDEC (Joint Electron Device Engineering Council) Solid State Technology Association standard, and solid-state drives. Solid-state drives offer better IOPS (input/output operations per second) for tablets than does the JEDEC standard but at a higher cost and power consumption (**Figure 1**).

Increasing performance and maintaining low power are the major challenges for memory designers, and many see universal flash storage, which accomplishes these goals, as the next big thing. Vendor support is weaker than it was when JEDEC first proposed the standard, according to Wong. As such, a solid-state drive with a low-power SATA (serial-advanced-technology-attachment) interface could be an alternative. "For example, the idle power of the SATA PHY [physical layer] is quite large," he says. "You could make it 'low power' by turning off the PHY when [it is] idle."

SETTING THE STANDARDS

JEDEC, a volunteer organization, sets open standards for the microelectronics industry and recently hosted a standardization meeting in Vancouver, BC, Canada, focusing primarily on memory-related topics. "The ongoing standards-development work within the JEDEC committees, focused on mobile memory, has significant strategic value to the industry and will help make possible a wide range of innovative new products," says Desi Rhoden, chairman of the JC-42 Committee for Solid State Memories. Published JEDEC standards that relate to mobile memory include LPDDR2 (low-power double data rate 2), universal flash storage, and *e*•MMC.

JEDEC designed the LPDDR2 JESD209-2E standard to enhance the design of mobile devices, such as smartphones, cell phones, PDAs (personal digital assistants), GPS (global-positioning-system) units, and handheld gaming consoles, by enabling increased memory density, improved performance, greater compactness, overall reduction in power consumption, and longer battery life. As a result, it offers advanced power-management features, a shared interface for nonvolatile and volatile memory, and a range of densities and speeds. The JC-42.6 Subcommittee for Low Power Memories published the standard in April 2009 and updated it in April 2011.

The JEDEC JESD220 universal-flash-storage standard targets both embedded and removable flash-memory-based storage in mobile devices that require high performance and low power consumption, such as smartphones and tablets. The standard uses the MIPI (Mobile Industry Processor Interface) Alliance's M-PHY (MIPI-physical-layer) and UniPro (Unified Protocol) specifications to form its interconnect layer. Because it combines this advanced interface with low active-power level and a near-zero idle-power level, universal flash storage shows promise in achieving significant reductions in device power consumption. JEDEC first published the standard in February 2011.

In June, JEDEC announced the publication of the JESD84-B45 Embedded Multimedia Card Electrical Standard Version 4.5, a low-cost data-storage and communication standard that targets applications such as smartphones, cameras, organizers, PDAs, digital recorders, MP3 players, pagers, and electronic toys. The latest version of the standard increases interface bandwidth from 104 Mbytes to 200 Mbytes to achieve high mobility, high performance, low power consumption, and high data throughput. This free standard helps to improve the interaction between the host processor and the memory device at the interface, configuration, and protocol levels to gain system performance and reliability (**Reference 2**).

LPDDR3 EXTENDS THE LPDDR2 STANDARD'S BANDWIDTH, REACHING 6.4 GBYTES/SEC, OR 12.8 GBYTES/SEC FOR DUAL CHANNELS.

JEDEC is also developing LPDDR3 to meet the higher bandwidth requirements of next-generation smartphones and tablets. JEDEC LPDDR3 effectively extends the LPDDR2 standard's bandwidth, reaching 6.4 Gbytes/sec and allowing 12.8 Gbytes/sec for a dual-channel configuration. It will support both POP (package-on-package) and discrete packaging types and preserve the power-efficient features and signaling interface of LPDDR2.

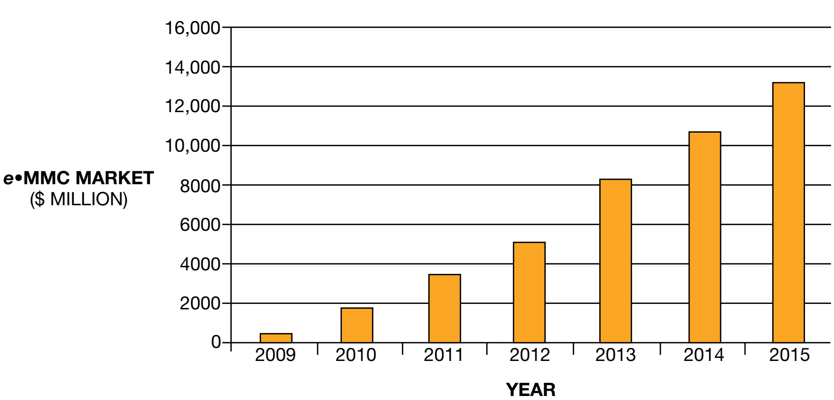

Figure 1 The *e*•MMC market, which includes smartphones and tablets, will continue to grow through 2015.

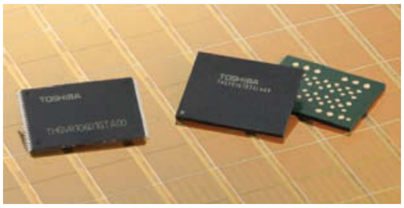

Figure 2 Toshiba's SmartNAND series integrates robust ECC and targets consumer mobile devices that require high-density, nonvolatile memory.

The JEDEC WideIO (wide-input/output) standard aims to satisfy industry demands for increased levels of integration and improved bandwidth, higher latency, lower power consumption, lower weight, and smaller form factor. JEDEC expects WideIO to provide performance, energy efficiency, and compactness for smartphones, tablets, handheld gaming consoles, and other high-performance mobile devices. WideIO mobile DRAM uses chip-level 3-D stacking with TSV (through-silicon-via) interconnects and memory chips on SOCs (systems on chips). WideIO will suit use in systems that require memory bandwidth as high as 12.8 Gbytes, including 3-D gaming, 180p high-definition video, and similar applications.

IN THE FIELD

Designers selecting mobile memory care about performance, form factor, and supply availability. According to Scott Nelson, vice president of Toshiba's memory business unit, NAND is the de facto storage medium for mobile memory because of density and low cost. He sees designers of mobile devices selecting NAND memory across a range of formats—from raw NAND, embedded memory with an embedded multimedia-card interface, to removable memory, such as SD (secure digital) and microSD.

One of the challenges for memory providers is the continuing need for improved error correction in next-generation NAND. In response, Toshiba offers an approach that addresses increasing needs for better ECC (error-correction code) and flash management. The company also offers the SmartNAND MLC (multilevel-cell) NAND product, which is essentially NAND with an ECC-controller chip (**Figure 2**).

Tetsuya Yamamoto, a Toshiba memory-engineer manager, observes that performance needs increase with each generation of JEDEC specification, which is an additional challenge. For instance, the most recent Embedded Multimedia Card specification raises performance

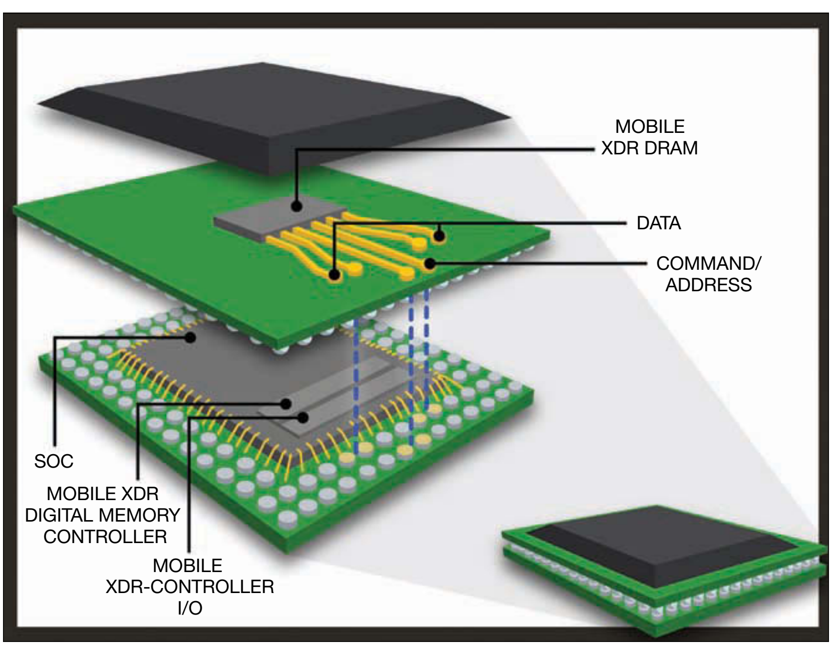

Figure 3 Rambus' Mobile XDR targets smartphones, netbooks, mobile gaming, and multimedia products.

FOR MORE INFORMATION

Forward Insights
www.forward-insights.com

IHS iSuppli Research
www.isuppli.com

Joint Electron Device Council Solid State Technology Association
www.jedec.org

Mobile Industry Processor Interface Alliance
www.mipi.org

Rambus
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SanDisk
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Toshiba
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to 200 Mbytes/sec. Yamamoto expects the universal-flash-storage standard to include a maximum speed of 2.9 Gbytes/sec. To address the performance issue, Toshiba plans to support a universal-flash-storage interface in addition to the one for the Embedded Multimedia Card.

According to Kendra De Berti, senior marketing manager for Rambus, the memory needs of smartphones and tablets represent a challenging mix, including low active and standby power, fast power-state transitions to increase battery life, small footprint, high bandwidth, multiple memory channels for high throughput, and the ability to support more powerful multicore processors. She notes that engineers must now create low-risk memory that uses and maintains backward compatibility with the infrastructure.

To address these challenges, Rambus has been building a patent portfolio for mobile memory with several proprietary technologies in the Mobile XDR (extreme-data-rate) memory architecture (**Figure 3**). For example, the company's low-swing differential-signaling technique delivers high data-rate performance at low voltage. Rambus has heavily invested in JEDEC's LPDDR2/3 standards, which use single-ended signaling, in which data and command/address signals are referenced to ground.

Rambus is closely following the emerging WideIO specification. "The promise of WideIO DRAM with TSV-interconnect technology is high bandwidth at low power in a compact footprint, and it would address the major shortcomings of the LPDDR, but it does so by introducing major issues of its own," says De Berti. She sees the need for significant development work before Rambus can supply WideIO with TSV technology with high yields and low costs. Further, she adds, significant changes to supply chains and business models will be necessary for broad adoption in mixed-IC, processor-plus-memory, implementations.

Figure 4 SanDisk's integrated solid-state drive offers fast, lightweight, and affordable storage for smartbooks, ultrathin PCs, and tablets.

The industry is also showing a lot of interest in solid-state drives for tablets (**Figure 4**). All of the major memory suppliers are also delivering new solid-state drives. "The real challenge is to provide increased performance and capacities at prices consumers want," notes Mike Wong, director of public relations for SanDisk Corp. "New mobile devices [are always] entering the market, and the sheer volume of products can be a challenge if developers are not prepared," he adds. EDN

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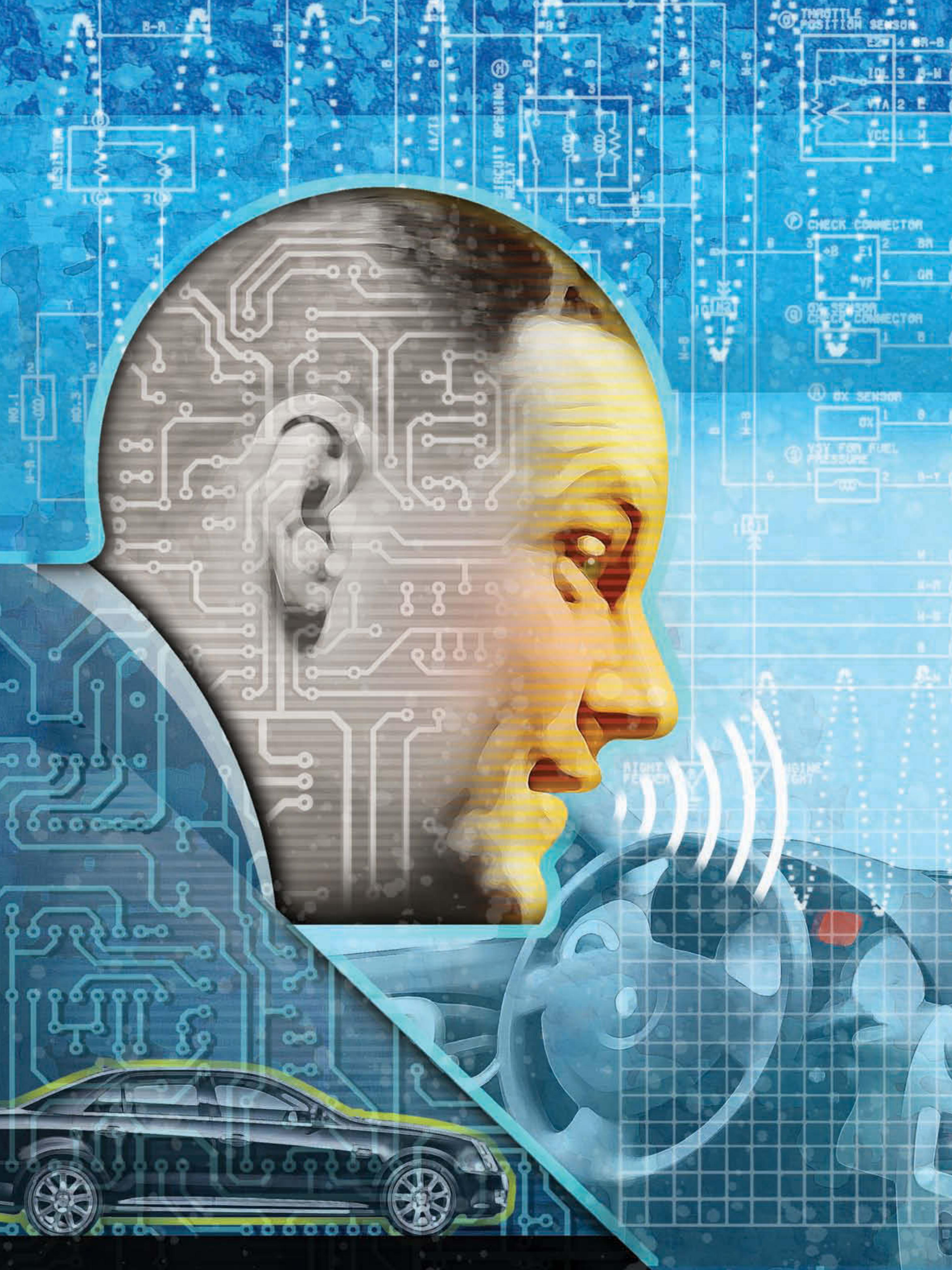
THROTTLE POSITION SENSOR
CHECK CONNECTOR
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VSV FOR FUEL PRESSURE
CIRCUIT OPENING RELAY
RESISTOR

VOICE RECOGNITION CUTS DRIVER DISTRACTION

DESIGN ENGINEERS SEE SPEECH-ENABLED USER INTERFACES AS VITAL TO IMPROVING AUTOMOTIVE SAFETY IN THE INCREASINGLY COMPLEX DRIVER COCKPIT.

BY RICK DEMEIS • EDITOR, AUTOMOTIVE DESIGNLINE

Since first appearing in automobiles in the late 1990s, voice-recognition user interfaces have grown in the breadth of their applications and in the quality of their performance. Realization of this utility fortunately comes at a time when drivers and passengers are bringing more and more personal electronic and connectivity devices into the car—with their potential for greater driver distraction. Burgeoning growth in vehicle systems and functions also presents increased potential for diverting driver concentration if the designers of these handheld devices do not plan well for feature interaction with the operator.

Developers are unanimous in agreement, however, that easy-to-use, intuitive speech recognition greatly reduces possible distractions by allowing drivers to keep their eyes—and attention—on the road and their hands on the steering wheel.

THE CHALLENGES

The automobile environment is not conducive to voice recognition, says Brian Radloff, director of worldwide embedded solution architecture for the mobile-speech division of Nuance Communications, a leading speech-recognition-software provider. The car is inherently noisy, and the need to use far-field microphones—at least in most applications—compounds the task.

IMAGE: GORDON STUDER

Figure 1 This head-unit display of a Ford Sync voice-texting screen visually depicts a few menu options.

When voice systems first appeared, he notes, the recognition rate was sometimes unacceptable. By the early 2000s, however, improvements in microphones, audio technology, and echo- and noise-cancellation and -subtraction algorithms moved recognition to where it needed to be. Other improvements included voice-recognition modules with built-in automotive-noise models, and modeling basic sound units of speech, or phonemes, in a vehicle's noise environment. "These [techniques] still form the core of our automotive offering today," Radloff adds.

AT A GLANCE

- Growing complexity in vehicles is forcing auto designers to rely on voice-recognition interfaces.
- Cars provide poor acoustic environments for voice recognition.
- Improvements in microphone technology and computing power help, but the algorithms remain challenging.
- The cloud and human assistance may play pivotal roles.

The availability of more processing capability enables more complex features, he says. For example, one improvement was the ability to "dial" a phone by saying the name of the target or by speaking the phone number's digits. Likewise, navigation performance in voice went from just zooming in and out on a map to inputting addresses by number, street, and town to the point at which users can just say the address in one phrase.

Today's speech-recognition systems can dynamically build vocabulary from the phone book in a user's phone, Radloff notes. In other words, the system automatically "reads" the phone-book listings and adds them to its vocabulary so that it can recognize them when the user speaks to dial a listed phone by name. Similarly, the systems can read music players to harvest song titles for later request by voice.

The latest MyFord Touch connectivity system with Nuance software uses both voice and touchscreen interfaces, incorporating many of these functions (**Figure 1**). "We are expanding the vocabulary with words, including synonyms, [to be even more intuitive]," says Radloff. An example would be responding to the words "I'm hungry" by composing a list of nearby restaurants. "The system combines processing power available, for [running] more robust algorithms and memory," he adds, and therein lies the rub.

PROCESSING POWER

Although software provides these functions, it requires a CPU hit to run, notes Radloff. Early voice-recognition systems ran using 100-MIPS processors. By the mid-2000s, that number had increased to approximately 500 MIPS, and today's more capable processors offer performance of 800 to 1500 MIPS. Radloff expects that this key enabling technology will reach 2500 MIPS by 2015. These numbers are more toward the trailing than the leading edge of processor development because developers must first make the devices robust enough for the temperature extremes and EMI (electromagnetic interference) of the taxing automotive environment.

So, what will automotive-speech-recognition technology be capable of with such power? Greater processing power will enable more natural language interfacing, says Radloff, using less-structured phrases, such as, "I want to hear Van Morrison." Further, new technology will enable 3G (third-generation) connectivity to the car and the off-board migration of some voice-recognition features to servers in the cloud

HYUNDAI GOES OFF INTO THE CLOUD—WITH HANDHOLDING

Hyundai is currently introducing its Blue Link telematics system with voice-recognition features that it partially based off-board the vehicle (Figure A). Hyundai and telematics-service provider ATX Group developed the system, which uses Nuance and Vlingo speech-recognition software.

The system marries speech recognition with agent assistance, says ATX's Don Tryon, senior director for account management at the company. Nuance software performs initial interactive voice recognition at a conversational pace. Vlingo tools, which have a large cloud-based library of utterances, analyze and monitor the response to the request for directions or a point of interest, for example. If the system has a confidence level on the order of 90% of the command, the function remains on the vehicle. If it falls below that level, an agent—using a list of Vlingo-provided options—talks to the driver for clarification and assistance.

Figure A With voice recognition, the physical interface for Hyundai's Blue Link telematics system is simple and clean.

The developers of Blue Link relied on development kits from software providers. "The sooner a system can be in the car for testing, the better," says Michael Deitz, senior group manager for Connected Car at Hyundai. The kits enable early checking of system performance in the actual vehicle's acoustic environment.

(see **sidebar** “Hyundai goes off into the cloud—with some handholding”). You can then run sophisticated applications, such as Nuance’s Dragon dictation for SMS (short-message-service) texting, which vendors are currently demonstrating and which should be operational in approximately 18 months. This technology sends a voice message to a server that then sends the text message.

By going off-board, voice recognition goes beyond the grammar-bound limitations of a fixed vocabulary, as with the memory and CPU limits of an embedded system in the car. SMS is general grammar that can have any combination of letters. So if you have the connectivity, you should take advantage of it, says Radloff, to do the needed processing off-board. Cloud-based service also updates navigation systems’ points of interest and construction-site data.

Also in the offing for the near term is the installation of more than one microphone, which allows more sophisticated noise cancellation and beam forming. Processing directs the “listening beam”—for instance by manipulating the delay of the same sound between microphones—to focus on the driver, lowering the tendency to pick up passengers’ voices.

MICROPHONE MANIPULATION

Scott Pennock, senior hands-free-standard specialist at the hands-free- and speech-technology division of QNX Software Systems, provides more insight into the subtleties of microphone installation. QNX partners with Nuance and provides acoustic-processing middleware in creating speech interfaces. One focus for QNX is the delivery of better voice signals to the speech-recognition system.

“Vehicle noise is diffuse—the same throughout the cabin,” Pennock says. “The challenge with the far-field microphones comes about because, if you double the distance to the speaker, you take a 6-dB hit in the SNR [signal-to-noise ratio].” Thus, it is better to install a microphone approximately 12 in. from the driver’s mouth rather than on the rearview mirror, which is approximately 24 inches away (**Figure 2**).

You derive another SNR benefit from adding another microphone for beam forming on the driver, he adds. But this improvement is only 3 dB because doing so raises the noise floor due to the fact that the second microphone picks up not only speech but also noise.

Another challenge that may not be obvious to speech-recognition developers is that systems have a required accuracy rate, but it can be daunting to determine whether the system has achieved that rate. This task was easier when systems used set commands rather than natural language. Now, however, systems must compete with natural

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ATX Group
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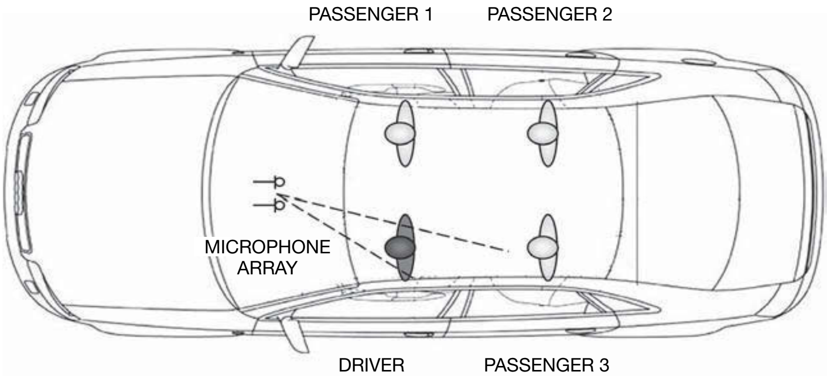

Figure 2 Two or more microphones using audio processing can form a sensitivity beam to pick up the driver's voice and reject sounds from the passengers talking in the background.

utterances as people speak normally.

Developers can perform testing with live subjects, which is time-consuming, and the samples of speech may be too small for today's increasing grammars to ensure that the technology adequately covers all accents, Pennock notes.

Nuance's Radloff says the company's speech-recognition systems come in 28 languages for automotive applications. These language models have built-in libraries of accents, such as US regional dialects. Algorithms in the recognition engine adapt to the speaker by learning from which system responses the user corrects. In contrast, developers of some early systems trained them to the user's voice by listening to a series of test words. This task would be time-consuming with today's extensive vocabularies.

A better approach is to build a library of utterances that developers can more efficiently play back. Developers should collect the utterances in a vehicle, in which people tend to talk louder and at a higher pitch. Interestingly, a person speaking a string of familiar phone-number digits in a natural cadence produces a higher recognition rate than one who is deliberately speaking slower, Pennock says.

Vendors of voice systems must test them under different operating conditions, ranging from a car that is idling to one traveling 70 mph with climate-control fans on high; during rain when the noise is not steady but a dynamically varying signal; and riding over louder concrete or quieter asphalt.

Good speech-recognition user-interface design is more than just high recognition rates, however. How a system recovers from errors must take into account both expert and novice users, notes Pennock. When the system does not recognize a phrase, it may prompt the user: "Did you say XYZ?" By detecting response pauses, the system can assume that the user needs more verbal prompts to perhaps learn phrases, whereas an experienced user will just confirm or repeat a request. The system then trains a user over time to become more expert.

With the multimode user interfaces available today, speech is most effective for putting more complex information into a user's head, such as requests for points of interest, audio selections, or phone calls, with more natural-language interaction without resorting to distracting touch scrolling. Users can effectively employ a simple action, however, to control climate or temperature with a quick touchscreen or switch stroke.

Brigitte Richardson, lead engineer for global voice-control technology and speech systems at Ford, notes that some fans of voice recognition want to expand its use for such functions as seat adjustments and window control—applications that familiar, basic switches now adequately handle. Users should instead become more aware of other functions that voice recognition enables (see **sidebar** "An embarrassment of riches").

One trend is apparent, however: Speech recognition is increasingly an enabler for interacting with new automotive features and user devices' connectivity, offering ease of use in a minimally distractive, safer manner. EDN

AN EMBARRASSMENT OF RICHES

When talking about the challenges of voice recognition, designers tend to think of SNRs (signal-to-noise ratios) and algorithms. Scott Pennock, senior hands-free-standard specialist at the hands-free- and speech-technology division of QNX Software Systems, however, notes that another hurdle is simply making users aware of speech-enabled features and functions—so that they can have a more pleasant and productive drive.

Brigitte Richardson, lead engineer for global voice-control technology and speech systems at Ford, echoes that thought. "People get into a car with so many features, such as traffic information, phones, and satellite and high-definition radio, but they don't know what you can control by voice," she says. "Likewise, they won't know what to say to give a command and interact with the car. People are reluctant to go through a system-given tutorial or read a large manual [as Ford provided in 2009]. Many users are unaware of weather radar or 'one-shot' destination entry [just by saying an address]."

Because of such tendencies, Ford and Nuance added more grammar with aliases—embedded synonyms to make the Sync system easier to access with minimal training. The overall adoption rate for Sync since its introduction in 2007, thanks to its features and utility, has been 79% across the Ford brand. The technology is complex, Richardson states, but that complexity is in the voice-recognition engine. Simplifying the user interface is key to acceptance and usability.

You can reach Designline Editor Rick Demeis at jldmld@comcast.net. Read more at www.eetimes.com/design/automotive-design.

BY JOHN BOTTRILL • TEXAS INSTRUMENTS

Discontinuous conduction brings issues to current-mode converters

A DESIGN THAT IS STABLE IN THE LAB MAY BECOME UNSTABLE AS OPTOCOUPLERS DEGRADE OVER TIME.

Control loops for power converters are complex and rely on the converter's operation within a window of defined conditions. However, when converters operate outside these defined conditions, they can exhibit unexpected behavior. This article explores one of the most common problems design engineers face: moving a forward buck converter from the normal defined operational window of continuous conduction into a light-load condition of discontinuous conduction.

You develop the control loop around a mathematical model of a buck converter (**Figure 1**). Established models exist for both current- and voltage-mode switching buck converters. For this model, you assume sufficient load current so that the current through the inductor is continuous. If you ignore losses and semiconductor voltage drops, the output voltage is equal to the input voltage factored by the turns ratio times the duty cycle. The primary-to-secondary turns ratio is 1-to-N. Ignoring diode and FET voltage drops, the voltage at the junction of the diodes when the switch is on is the input voltage times N.

You now increase the load impedance to the point that the current through the output inductor is no longer continuous. Your basic assumption is then no longer valid. In this case, the control theory that relates to the continuous model is inaccurate, and the converter begins discontinuous operation, during which the current moving through the inductor to the output is discontinuous. The output inductor sometimes does not connect to the transformer winding or to ground through a diode. When the primary-side switch is on, the current through the output inductor increases linearly. The slope is a function of the voltage across the inductor. When the switch turns off, the current through the inductor tries to continue, causing the voltage to drop and pulling current through the diode that connects to ground. With the reversal of voltage across the inductor, the current through the inductor starts to decrease. In discontinuous operation, the current falls to 0A.

The average current in the output inductor must equal the load current. You can write a series of **equations** to define the circuit in continuous mode. First, ignore diode and FET-switch voltage drops. When the FET is on, the voltage at the input to the output inductor, L_{OUT}, is $V_{IN}\times N$. You can then define the output as a function of input voltage; duty cycle, D; and transformer turns ratio, N:

$$V_{IN}\times N\times D=V_{OUT}.$$

You can now calculate the peak current through the inductor:

$$I_{PK}=I_{DC}+0.5\times\frac{L_{OUT}}{(V_{IN}\times N)-V_{OUT}}\times\frac{D}{F_{SW}},$$

where F_{SW} is the switching frequency. The integral of the current through the inductor must equal the total load current for the cycle, thus preventing a net change in the output voltage.

In a continuous-current-mode forward converter, a slight change in the inductor current accumulates over the total cycle time, changing the charge that the converter transfers to the output. In discontinuous operation, the change in current has less effect because it conducts for only a small percentage of the time, resulting in a change to the gain of

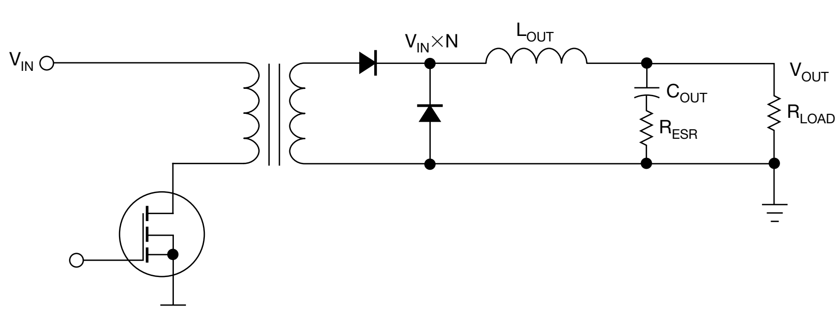

Figure 1 In this model of a forward converter, you assume continuous current through the inductor and ignore losses and semiconductor voltage drops.

the circuit and a change in the circuit dynamics. You use a different mathematical model to represent discontinuous-converter operation.

You can plot the output impedance of the converter over frequency for two load values (**Figure 2**). Given the assumed circuit values, the converter remains in continuous-conduction mode. Once you select a turns ratio for the transformer and a control IC, you can design the control loop, which has a gain from your theoretical control to the output voltage. You can chart that gain over frequency for both load conditions (**Figure 3**).

You should design the output-to-control feedback loop so that the gain will be one at your desired crossover frequency. The slope of the gain at this point of the gain curve is 20-dB—a factor-of-10—roll-off per decade. If you chose a crossover at 5 kHz, the control-to-output gain is 0.5, meaning that your feedback loop should have a gain of two at 5 kHz.

First, establish the feedback components from the control IC's COMP pin back to the sensor/amplifier. You must take into account the range of voltage that the COMP pin requires. This portion requires a constant gain of four. The error-amplifier sensor circuit must have a gain of 0.5 at 5 kHz, and the gain should be nearly flat at 1 and 25 kHz. You tailor the gain shape around the error amplifier (**Figure 4**).

YOU CAN PLOT THE LOOP GAIN OVER FREQUENCY FOR THE OPTOCOUPLER'S EXTREME AND NOMINAL CURRENT-TRANSFER RATIO.

The optocoupler and other circuitry must multiply the gain by a factor of four to compensate for the 0.5 gain of the error amplifier at 5 kHz. You accomplish this task by setting a gain of two through the optocoupler and two in the internal error amplifier in the PWM (pulse-width-modulation)-controller IC.

The optocoupler model employs real devices that have current-transfer-ratio variations of 50 to 200%. You can plot the loop gain over frequency for the optocoupler's extreme and nominal current-transfer ratios (**Figure 5**). You plot the phase shift of the loop to verify the stability of the converter (**Figure 6**). The converter has more stability if it has more than 40° of phase margin when the loop gain crosses one.

Figures 1 through **6** represent stable operation using a model with continuous current through the output inductor. When the load decreases, the inductor current becomes discontinuous. The high-frequency impedance of the converter remains the same, but the low-frequency impedance increases (**Figure 7**). If the dc-load resistance increases to 50**Ω**, the converter supplies a current of 0.2A.

For each cycle of a converter operating at 100 kHz, the load requires a 2-μC charge, Q. This charge arrives at the output in the form of a triangle of current with a definable upward slope based on the input voltage's turns ratio, the output voltage, and a definable downward slope based on the output voltage (**Figure 8**). Because the current peak is com-

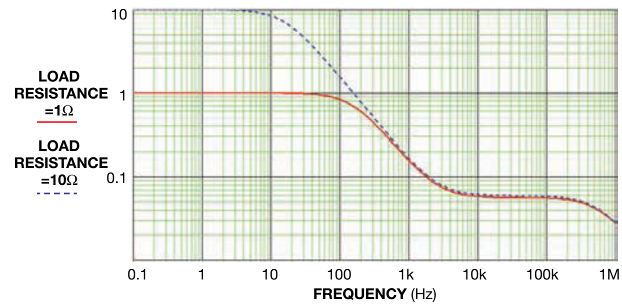

Figure 2 The output impedance over frequency of a converter in continuous-conduction mode changes with different output loads.

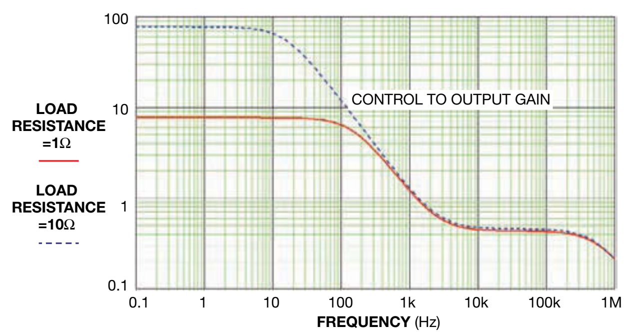

Figure 3 The gain over frequency from the COMP pin to the output voltage changes with applied load.

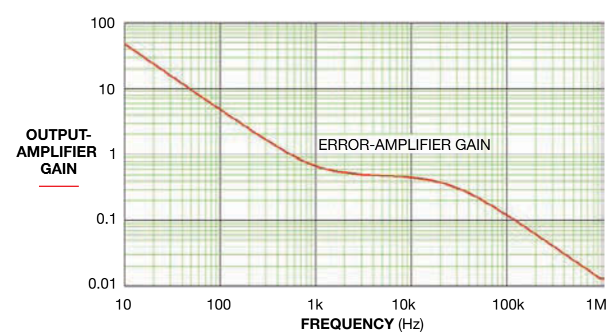

Figure 4 The error amplifier in the regulator IC has changing gain as a function of frequency.

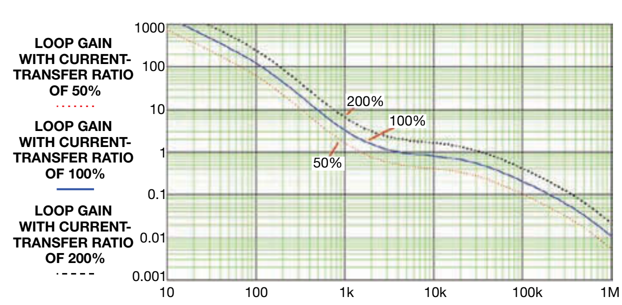

Figure 5 The open-loop gain of the converter varies depending on the current-transfer ratio of the feedback optocoupler.

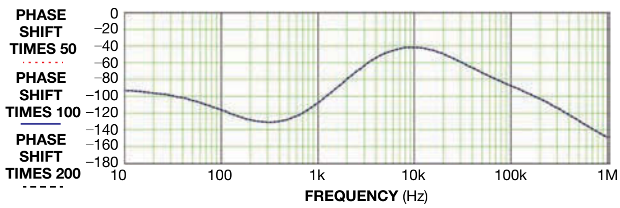

Figure 6 The open-loop phase shift of the converter remains the same over the feedback optocoupler's three current-transfer ratios.

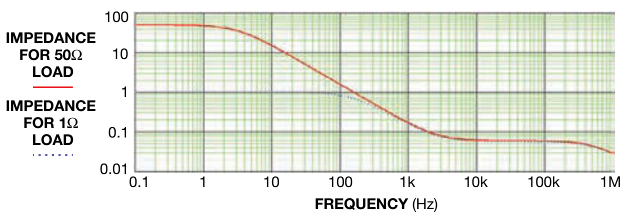

Figure 7 With a light load, the output impedance over frequency rises at low frequencies.

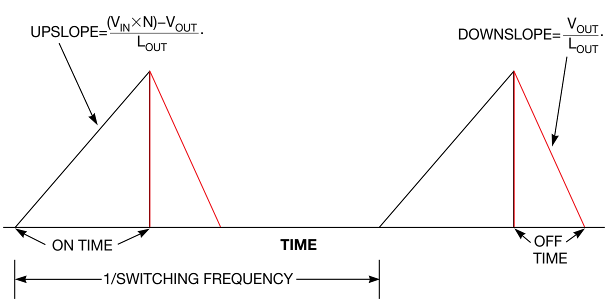

Figure 8 In discontinuous-conduction mode, the inductor's current waveforms decrease to 0A.

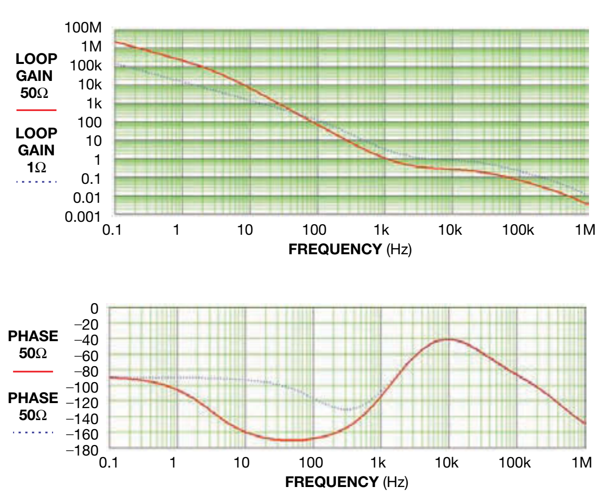

Figure 9 In discontinuous-conduction mode, the open-loop gain and phase of the converter change substantially.

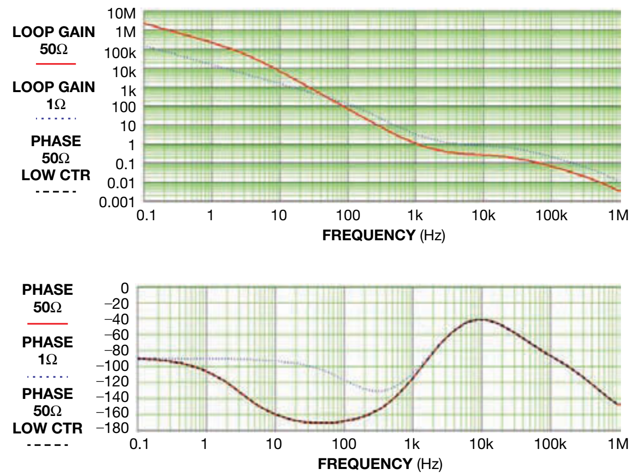

Figure 10 If the optocoupler's current-transfer ratio is low, the converter might become unstable under light loads when it enters discontinuous mode.

mon and a function of the on time, the upward and downward slopes are ratios of each other.

Again, ignore diode and FET voltage drops. You can relate the off time to the on time and the slopes with the following **equation**:

$$T_{OFF}=\frac{T_{ON}\times UPSLOPE}{DOWNSLOPE},$$

where T_{OFF} is the off time, T_{ON} is the on time, UPSLOPE is the upward slope, and DOWNSLOPE is the downward slope. You can use this **equation** to determine Q, the charge per cycle:

$$Q=\frac{I_{OUT}}{F_{SW}}=0.5\times UPSLOPE\times T_{ON}\times(T_{ON}+T_{OFF})=\frac{0.2A}{F_{SW}}=2\ \mu C.$$

You define the upward slope by relating the input voltage, the turns ratio, and the output voltage:

$$UPSLOPE=\frac{V_{IN}\times N-V_{OUT}}{L_{OUT}}=\frac{\frac{75V}{N_{PRI}}-10V}{L_{OUT}}=0.429A/\mu SEC,$$

where N_{PRI} is the reciprocal of the transformer's primary turns. The downward slope of the inductor current depends on the output voltage and the inductor value:

$$DOWNSLOPE=\frac{V_{OUT}}{L_{OUT}}=\frac{10V}{L_{OUT}}=0.13A/\mu SEC.$$

You can combine the above **equations** and rearrange them to solve for the on time:

$$T_{ON}=\sqrt{\frac{2\times Q\times DOWNSLOPE}{UPSLOPE\times(UPSLOPE\times DOWNSLOPE)}}=1.476\ \mu SEC.$$

From these **equations**, you can calculate the peak secondary-side current:

$$I_{PK}=T_{ON}\times UPSLOPE=0.632A,$$

where I_{PK} is the peak current. Because you have chosen a turns ratio, you can infer the primary-side peak current. This secondary peak current translates to the primary side through the power transformer and the current-sense transformer to the current-sense resistor. (You can access a detailed schematic of this design from the Web version of this article at www.edn.com/ms4398.) With a UCC2813-2 controller, it represents a voltage of 1.435V on the COMP output. This voltage includes offsets and internal IC gain. You next remove any offsets to identify the contribution of the current within this voltage. The portion of the COMP voltage due to the peak current is 0.085V.

TEST THE STABILITY OF THE UNIT UNDER MINIMUM-LOAD CONDITIONS IN CASE ANY ISSUES ARISE.

The dc gain of the control to the output is the output voltage divided by the primary current-sense voltage. In this case, the output voltage is 10V; divided by the peak current, it yields 0.085V, or 117.255V. You can now determine the complete open-loop gain and phase (**Figure 9**). This figure includes the gain of the error amplifier as well as that of the other circuit parameters. The change in output load changes the loop gain as well as the phase response.

In this converter design, the loop 0-dB gain-crossover frequency decreases from 5 kHz with approximately 120° of phase margin to a 0-dB gain-crossover frequency at 1 kHz and 60° of phase margin. With this design, the converter is stable under both conditions, but the change is significant.

Now consider a case in which the current-transfer ratio of the optocoupler is low (**Figure 10**). The 0-dB loop crossover is 600 Hz, and the phase margin is 45°. This marginal amount means that the control loop is still stable. The variable parameter of current-transfer ratio might mean that a design that is stable under normal continuous operation will have problems in discontinuous mode. As the current-transfer ratio of the optocoupler degrades over time, your designs could have problems in discontinuous mode. You should test the stability of the unit under minimum-load conditions in case any unexpected issues arise with the discontinuous current through the output inductor. Build your designs with margins to handle these conditions. **EDN**

AUTHOR'S BIOGRAPHY

John Bottrill is a senior applications engineer at Texas Instruments (Manchester, NH), where he supports customers and evaluates new ICs before release. In doing so, he has produced more than 20 technical papers and has two patents to his credit. He received a bachelor's degree in electrical engineering from Queen's University (Kingston, ON, Canada).

Positive edges trigger parabolic timebase generator

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Nonlinear systems often need to become linear to be useful, and the circuit in **Figure 1** provides a nonlinear sawtooth pulse for a PWM (pulse-width modulator) that can compensate for nonlinearities in sensors, controllers, or systems. The circuit outputs a linear sawtooth pulse, a quadratic parabolic pulse, and a cubic parabolic pulse of equal and constant width following an external trigger pulse. All pulses have equal peak amplitudes.

The circuit incorporates a cascade of three synchronously switched integrators. IC$_3$'s S_2D_2 switch switches the input of integrator IC$_{2D}$, the first in the chain, to the source of reference voltage V_{REF}. You need two integrators employing IC$_{2D}$

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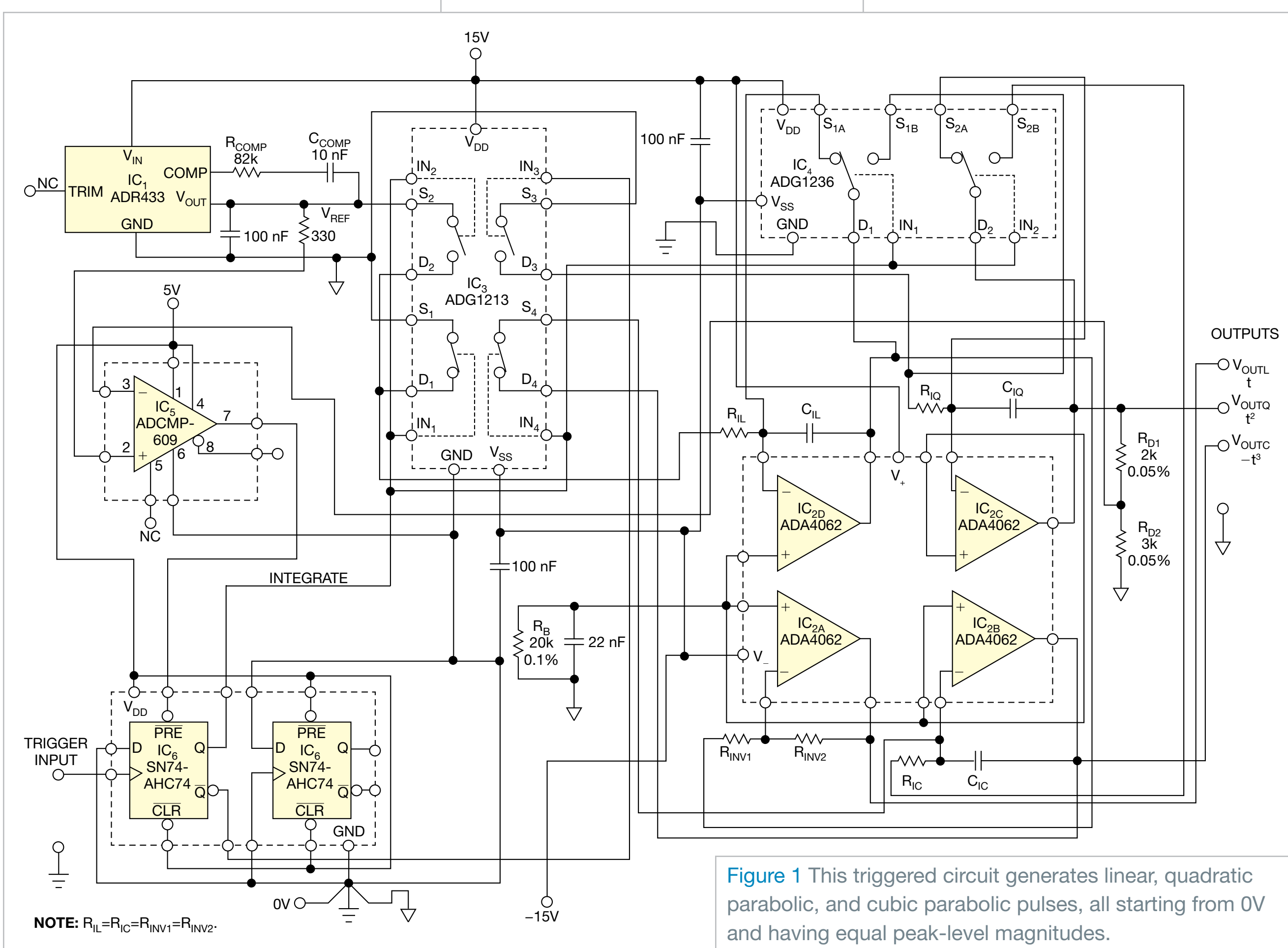

Figure 1 This triggered circuit generates linear, quadratic parabolic, and cubic parabolic pulses, all starting from 0V and having equal peak-level magnitudes.

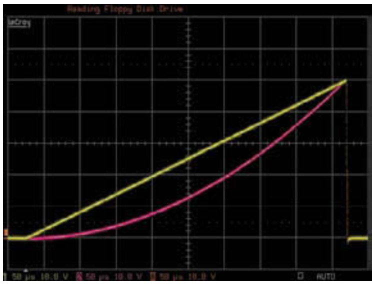

Figure 2 At the midwidth of the pulse, the quadratic parabolic pulse's voltage level (pink trace) is exactly one-fourth of its peak level.

and IC_{2C} to generate a quadratic parabolic pulse. The third integrator, using IC_{2B}, lets you simultaneously generate a cubic parabolic pulse. Each integrator has a series input switch and a reset switch that connects in parallel with a respective integrating capacitor.

The $S_{1A}D_1$ switch in IC_4 is a reset switch for integrator IC_{2D}. The complementary $S_{1B}D_1$ switch serves as a series input switch for integrator IC_{2C}. Similarly, the $S_{2A}D_2$ switch is a reset switch for integrator IC_{2C}. The $S_{2B}D_2$ switch is a series input switch for integrator IC_{2C}. The positions of all switches are at logic high at all control inputs: IN_1 to IN_4 of IC_3 and IN_1 and IN_2 of IC_4.

Integrators IC_{2D} and IC_{2C} also have input-grounding switches in IC_3, S_1D_1, and S_3D_3, respectively. The grounding switches ensure that error due to leakage currents of the series switches is approximately 50% less than that of a design not using the grounding switches.

The Integrate logic signal controls all series switches. When the signal is high, it turns on all the reset and grounding switches. Thus, integrators IC_{2B}, IC_{2C}, and IC_{2D} are either integrating their respective analog input signals or resetting to a 0V output. The input of integrator IC_{2D} switches to the output of precision voltage-reference cell IC_{2A}. Thus, signal V_{OUTL} becomes a negative sawtooth pulse. The pulse varies within its duration, T_1, as:

$$V_{OUTL}(t)=-V_{OUTLPEAK}\times\frac{t}{T_1}.$$

Inverter IC_{2A} inverts this pulse. IC_{2A} has a voltage gain of negative one because positive pulses are more common. Integrator IC_{2B} integrates sawtooth pulse V_{OUTL}; IC_{2B} therefore outputs a quadratic parabolic pulse:

$$V_{OUTQ}(t)=V_{OUTQPEAK}\times\left(\frac{t}{T_1}\right)^2.$$

The **equation** describes a pulse that integrator IC_{2B} simultaneously integrates, producing a cubic parabolic pulse:

$$V_{OUTC}(t)=-V_{OUTCPEAK}\times\left(\frac{t}{T_1}\right)^3.$$

$V_{OUTLPEAK}$, $V_{OUTQPEAK}$, and $V_{OUTCPEAK}$ are negative or positive voltage peaks at the outputs of their respective integrators. T_1 is the width of the Integrate pulse. Theoretically, to achieve $V_{REF}=V_{OUTLPEAK}=V_{OUTQPEAK}=V_{OUTCPEAK}$, you must stagger the integrating time constants of the respective integrators as 1-to-1/2-to-1/3, respectively. In this case, however, V_{REF}=3V, whereas $V_{OUTLPEAK}=V_{OUTQPEAK}=V_{OUTCPEAK}$=5V.

You must multiply the 1 in the staggering ratio by 3/5. Considering the time constant of integrator IC_{2C}, you get a stagger ratio of 6/5-to-1-to-2/3. For the equal values of integrating resistors $R_{IL}=R_{IQ}=R_{IC}$, this staggering holds true for the values of respective integrating capacitors. The circuit uses a high-quality, SMD (surface-mount-device) ceramic capacitor, C_{IQ}, with a value of 2.3692 nF. To achieve the necessary precision staggering, C_{IL} comprises 2.4016-nF, 343-pF, and 79-pF capacitors in parallel. C_{IC} is a parallel combination of 1067 pF and 499 pF.

A rising edge at the trigger input forces the Integrate signal low, which turns off the reset and grounding switches and turns on the series switches. The integration lasts until $V_{OUTQPEAK}$=5V, forcing the output of IC_5 low, which in turn sets Integrate high. Thus, the series switches are off, and the reset and grounding switches are on. The circuit remains in this steady state until the next rising edge at the trigger input. The Analog Devices (www.analog.com) ADG1213 and ADG1236 switches work well in this design because of their charge injection of 1 pC or less. **Figure 2** shows the circuit's high precision, depicting linear and quadratic-parabolic-pulse shapes. EDN

Measure small currents without adding resistive insertion loss

Maciej Kokot, Gdansk University of Technology, Gdansk, Poland

In most cases, you measure current by converting it into a proportional voltage and then measuring the voltage. **Figure 1** shows two typical methods of making the conversion. In one method, you insert a probing resistor, R_P, in series with the current path and use differential amplifier IC_1 to measure the resulting voltage drop (**Figure 1a**). A second method is a widely known operational amplifier current-to-voltage converter in which inverted IC_1's output sinks the incoming current through the feedback resistor (**Figure 1b**).

In the first method, the same current that flows into one node flows from the second node, but a significant voltage drop occurs across probing resistor R_P. In the second method, the voltage drop is on the order of tens of microvolts to millivolts, depending on IC_1's quality, but the measured current flows only into the sensing node with no return to the circuit. You can measure only currents flowing to ground.

The circuit in **Figure 2** operates in a somewhat similar manner to the one in **Figure 1b** in that an op amp's output sinks the incoming measured current. However, the other op amp's output sources an equal outgoing current back to the circuit under test.

In **Figure 2**, input current I flows through R_1 into the output of IC_2, which reduces its voltage by the amount of IR_1 relative to the input node. That voltage equals the voltage mean of the op amp's outputs, which R_3 and R_4 set at the op amp's inverting inputs. Consequently,

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the output of IC_1 must rise to a voltage of IR_2 relative to the inverting inputs and the equal-voltage noninverting input node of IC_2. IC_1 sources this current, which returns through R_2 to the circuit under test. $R_1=R_2$, so the output current is the same as the input current. Because the op amp's outputs maintain their inputs at equal voltages, the circuit under test has virtually no resistance.

The circuit in **Figure 2** has the advantages but not the drawbacks of those in **Figure 1**. The current that flows into the first node flows from the other node, and the voltage drop is almost zero; the maximum is twice the input offset voltages. You can use this circuit in a circuit under test without changing the voltage and current flows. **EDN**

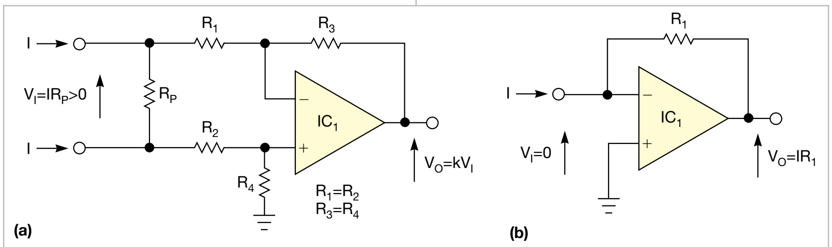

Figure 1 In one method of converting current to a proportional voltage, you insert a probing resistor, R_P, in series with the current path and use differential amplifier IC_1 to measure the resulting voltage drop (a). In another method, inverted IC_1's output sinks the incoming current through the feedback resistor (b).

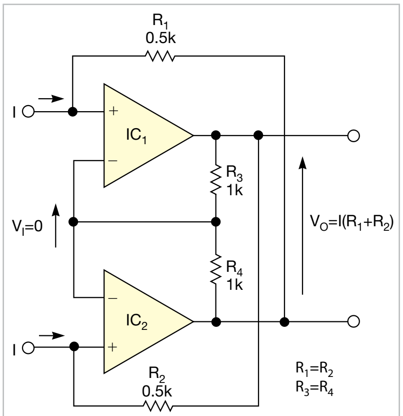

Figure 2 This current-to-voltage conversion method forms a zero-voltage converter.

Power resistor varies in value

Bogdan Raducanu, Bucharest, Romania

Testing power supplies or discharging batteries usually requires a constant-current load. Sometimes, however, you must study the behavior when the load is a resistor. Using a high-power potentiometer is an expensive approach that might not be worth the cost. The circuit in **Figure 1**, which performs like a high-power resistor that connects between P_1 and P_2, provides an alternative approach.

To understand how the circuit works, assume that the op amp is ideal and that the total resistance of R_2 and R_3 exceeds that of a high-power resistor (not shown). R_2 and R_3 form a divider that produces an output voltage, according to the following **equation**:

$$V_{REF}=V_{IN}\frac{R_2}{R_2+R_3}.$$

The operational amplifier maintains a voltage, such that R_1's voltage equals the reference voltage, that causes the current through R_1 to be:

$$I_{R_1}=\frac{V_{R_1}}{R_1}=\frac{V_{REF}}{R_1},$$

Substituting the first **equation** in the second **equation** yields:

$$I_{R_1}=\frac{V_{IN}\dfrac{R_2}{R_2+R_3}}{R_1}=V_{IN}\frac{R_2}{R_1(R_2+R_3)}.$$

If you neglect the current through R_2 and R_3, then R_1's current equals the input current, as the following **equation** describes:

$$I_{IN}=V_{IN}\frac{R_2}{R_1(R_2+R_3)}.$$

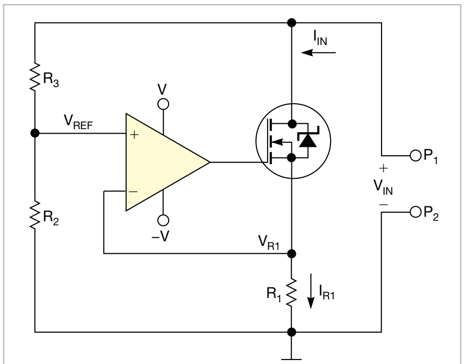

Figure 1 The resistance of the MOSFET, functioning as a variable resistor, changes.

This **equation** shows a linear relationship between the input current and the input voltage. Thus, the circuit between P_1 and P_2 acts as a resistor. The **equation** then becomes:

$$R=\frac{V_{IN}}{I_{IN}}=R_1\frac{R_2+R_3}{R_2}=R_1k.$$

where $k=(R_2+R_3)/R_2$ is a factor greater than 1, which multiplies R_1. Making either R_2 or R_3 variable lets the circuit function as a variable resistor. The cost of a suitable transistor and R_1, along with the rest of the components, is smaller than that of a variable potentiometer that can dissipate the same amount of power.

The circuit has some limitations, however. First, it can accept input voltages

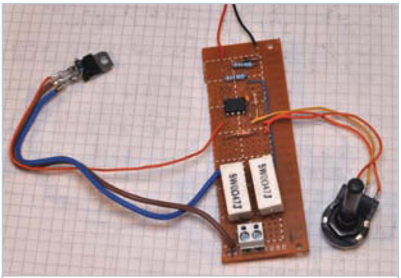

Figure 2 It is easy to assemble the circuit on a prototype board.

of only one polarity, which might limit its use in some applications. Second, the minimum resistor value is the value of R_1 plus the transistor's minimum on-resistance. Other factors such as op-amp offset, the values of R_2 and R_3, and input voltage influence the circuit's linearity, but the circuit still achieves high performance with low-cost components. Depending on the op amp's input range, the circuit requires an external dual power supply. **Figure 2** shows a prototype of the tested and built circuit using a potentiometer for changing the equivalent resistance and no heat sink on the power transistor. EDN

Minimize noise in power-supply measurements

John Lo Giudice, STMicroelectronics, Schaumburg, IL

You must minimize noise when measuring ripple in power rails because the ripple's amplitude can be low. Oscilloscope probes are essential measurement tools, but they can introduce noise and errors. Ground leads, such as those that attach to standard oscilloscope probes, can add noise that's not present in your circuit to an oscilloscope's trace. The wire loop acts as an antenna that picks up stray magnetic fields. The larger the loop area, the more noise it picks up. To prove this theory, connect the oscilloscope ground lead to the probe tip and move it around. The oscilloscope will show the noise increasing and decreasing with the ground-lead movement. You can use an oscilloscope probe with its ground lead and sockets to build a simple interconnect board (**Figure 1**).

Start by removing the probe's cover, which reveals the probe tip. There is a short distance between the tip and the ground ring. You need one of two sockets: a right-angle, or horizontal, socket or a vertical socket, similar to those in **Figure 1**. Solder the center leg of the socket to the output of the power supply and solder the other leg to the power-supply return. Connect a 0.1-μF surface-mount, stacked ceramic capacitor between the two sockets. This step limits the probe bandwidth to approximately 5 MHz, which further reduces high-frequency noise and lets the lower-frequency ripple pass through. **Figure 2** shows the completed interconnect board, and **Figure 3** shows a schematic of the board. Insert the probe tip into the socket to measure ripple. You will get a ripple measurement without spikes or other noise.

You should use a multilayer stacked ceramic capacitor because it's better at decoupling high-frequency noise. Electrolytic, paper, and plastic-film capacitors comprise two sheets of metal foil. A sheet of dielectric separates the metal-foil sheets, and these three components form a roll. Such a structure has self-inductance; thus, the capacitor acts more like an inductor than a capacitor at frequencies higher than a few megahertz. **Figure 4** shows the impedance to the power supply for various stacked-ceramic-capacitor values. EDN

Figure 1 A standard oscilloscope probe has a ground lead that can pick up noise.

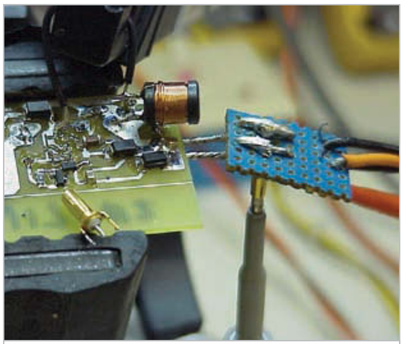

Figure 2 Solder wires from the power supply under test to an interconnect board reduce ground-lead length.

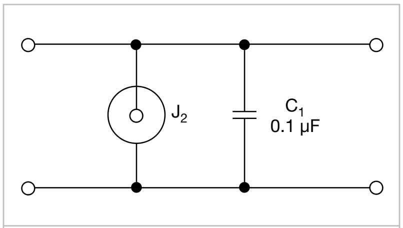

Figure 3 A ceramic capacitor further reduces high-frequency noise.

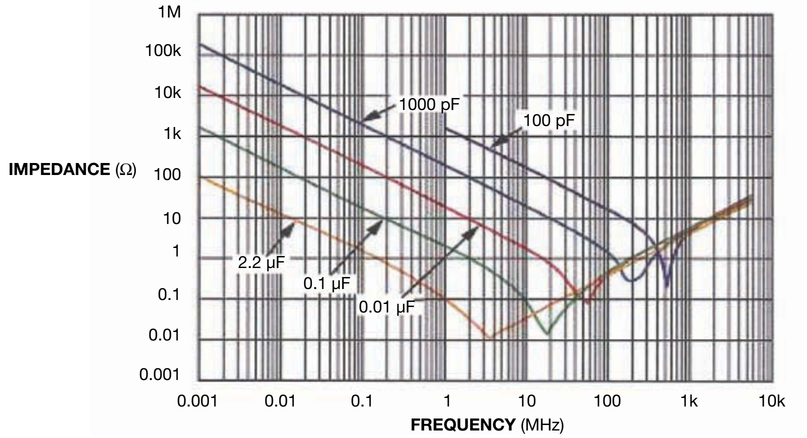

Figure 4 Probe impedance varies with capacitor value.

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The VPT series of transformers uses toroidal construction, which inherently helps reduce stray fields, increases efficiency, and minimizes size. The transformers are constructed with a Class B, UL-approved insulation system rated for 130°C, which provides 4000V primary-to-secondary isolation. The transformers operate over 25 VA to 2.5 kVA and feature an input voltage of 115/230V ac at 50/60 Hz and an output voltage of 6 to 230V. Voltage regulation is as much as 2.5% from full load to no load. The devices come in packages ranging from 71 to 208 mm in diameter, 32 to 112 mm in height, and 0.4 to 19.4 kg in weight, depending on model. Prices start at $12 (100).
Triad Magnetics, **www.triadmagnetics.com**

Power inductors improve dc resistance

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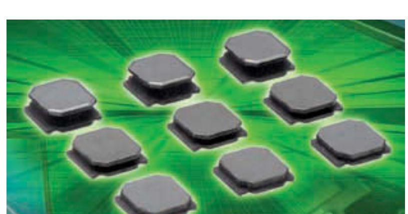
Taiyo Yuden Co Ltd,
www.t-yuden.com



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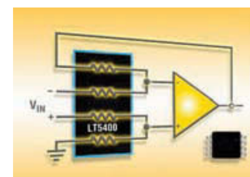
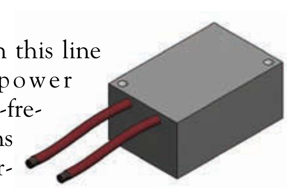


Linear Technology Corp,
www.linear.com

Small power inductors target high-frequency systems

Inductors in this line of high-power inductors for high-frequency applications use gapped amorphous ribbon cores and are thus 30% smaller and lighter than inductors using conventional silicon-steel or powdered-iron cores. The inductors combine high inductance and current levels with low losses at frequencies of approximately 20 kHz. The



box-shaped inductors are fully encapsulated in black epoxy resin, and they have a Class F insulation system. The two leads exit from the short end. Inductance values range from 100 to 500 μH, and current ratings are as high as 60A. Prices start at $25.
Alpha-Core Inc,
www.alphacoredirect.com

Inductors feature inductance values of 0.22 to 10 μH

The IHLP line of inductors comes in a 3232 case size and features an 8.18×8.64-mm footprint and a 4-mm profile. The IHLP-3232DZ-01 offers maximum dc resistance as low as 1.68 mΩ and a range of standard inductances from 0.22 to 10 μH. The device has a frequency range as high as 5 MHz, a saturation current of 9 to 34A, a heat-rating current range of 5.2 to 30.7A, and maximum dc resistance of 1.68 to 59.9 mΩ. The inductor handles high transient-current spikes without hard saturation and operates at −55 to +125°C. The device sells for 30 cents each (10,000).

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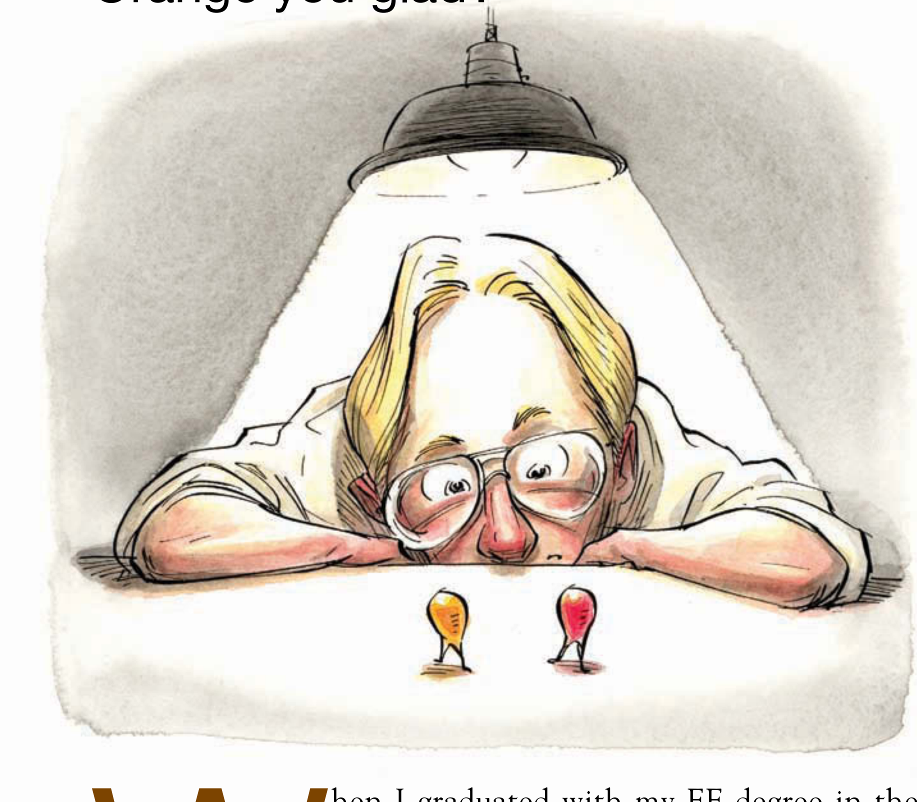

When I graduated with my EE degree in the ancient days of the mid-1970s, I quickly began to find out how much I didn't know. In the classroom, a capacitor was a capacitor, you knew the LaPlace and Fourier transforms, and you probably could even come up with the formula for how a capacitor charges. In the real world, though, especially in the through-hole days, capacitors were bewildering arrays of dielectrics and big packages.

About that time, I also learned that the most valuable people to know in your company were the final-test technicians. They had to figure out all the work-arounds and troubleshooting to make the product work after it went out the door.

The engineering department often was unaware of what the products they designed were doing out there in the world. My alliance with the testing department began simply as an engineer helping out, but it evolved into a friendly contest of challenges from the technicians—problems that I needed to solve.

One of those challenges involved capacitors. In those days, it was difficult to obtain hard copies of diagnostic data, so many of our products involved chart recorders. These required data for the X and Y axes, as well as intensity data, so we dedicated multiple through-hole PCBs (printed-circuit boards) to driving these monstrosities. Even though it was neither my responsibility nor my product, the final-testing guys called on me when they were running out of options for a PCB that ran the chart recorder.

At first, the only thing I knew was that they were running out of the "good" red capacitors. The team was routinely changing one capacitor on a board; otherwise, the board would not pass spec. The part in question was a huge, 47-µF, 20V orange-teardrop tantalum capacitor. When I examined the schematic, I was surprised about where this capacitor resided in the circuit. The 1-kHz ramp that drove the X of the chart recorder ran through a section of the circuitry that amplified the ramp but not any dc offset. The gain amp amplified the ramp through a front-panel potentiometer, acting as a magnification on the recorder.

The original designer did not want the signal to move off-screen when the gain increased, so the offset had to be as small as possible. He met this goal by using an architecture in which the ramp signal traveled to the noninverting input of an op amp. The gain resistor comprised a resistor and a capacitor—my orange buddy—in series, connecting to 15V. The designer was using a capacitor in that position so that the dc component had unity gain and the 1-kHz ramp received amplification. Due to the low frequency, the designer used a large, polarized capacitor, so he tied the positive end to the 15V rail.

A spec described how far, dc-wise, the ramp could move when we moved the front-panel potentiometer from one extreme to the other. With the good old red capacitors, every board passed. With the new orange parts, about half failed, at which point the technicians replaced the orange ones with red ones. The reason for the change in capacitors was simple—the orange ones were cheaper.

The next step was to grasp the difference between the capacitors. I read up on tantalum capacitors. Data was more difficult to come by in those days than it is today; you had to either order it through the mail or get a salesman to bring it to you. Nevertheless, I acquired the information, and I soon discovered specifications on leakage, specifically that leakage varied with bias. I went back to the test technicians and asked one of them to grab one of the "bad" boards.

Because there was 5V on the board, I asked the tech to cut the 15V land and rewire the cap to 5V. Instant success! The board not only passed testing but also looked better than the boards with the good capacitors. EDN

Steve Tomporowski, an analog engineer for more than 35 years, currently works at Kaman Precision Products.

DANIEL VASCONCELLOS

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